Soldering and Mounting Techniques

Reference Manual

SOLDERRM/D
Rev. 6, September−2008

ON Semiconductor®

PUBLICATION ORDERING INFORMATION

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Section 1

General Pb (Lead) Free Lead Finish/ Plating Strategy

General Pb (Lead) Free Lead Finish/Plating Strategy

In order to provide maximum flexibility and convenience for our customers, ON Semiconductor is modifying its strategy to support the Pb−free global initiatives from the previous General Announcement #12770.

Pb−free Plating Strategy − ON Semiconductor now offers a portfolio of devices that are plated with Pb−free lead finishes. Many of our products were originally released as Pb−free and do not have a comparable leaded version available. For devices which have been Pb−free since their inception, we do not intend to introduce any new Pb−containing lead finish versions of those devices.

For those customers that choose not to convert to our Pb−free offering according to our conversion plan, ON Semiconductor will continue to offer the current Pb containing devices until business conditions no longer prove feasible. We are committed to meeting the needs of all of our customers as our industry transitions to Pb−free over the next couple of years.

ON Semiconductor has qualified the majority of our packages in the Pb−free version and have made them available for sampling and production ordering. The list below shows the packages that have been qualified and the few remaining with their targeted completion dates. Please contact your ON Semiconductor Sales Representative if this schedule does not meet your conversion needs, or if you want to order Pb−free samples.

ON Semiconductor is fully compliant with the RoHS directive for all of the parts for which it makes business sense to do so. In other words, ON Semiconductor offers Pb−free versions of all of the parts for which there is sufficient demand. We will also continue to offer all of these parts in a standard Tin−Lead (SnPb) lead finish until market conditions necessitate a change in direction.

Moisture Sensitivity Level (MSL) − Surface Mount Packages are qualified to 260°C, which is compliant to the JEDEC standard J−STD−020C. The majority of the MSL ratings will remain unchanged from the current MSL 1 classification. If there is a change in the MSL rating of a package, the customer will be notified and appropriate packing precautions will be taken before any product is shipped by ON Semiconductor.

Product Identification − Devices offered without a Pb containing lead finish will be concatenated with a "G" suffix to denote Pb−free lead finish and qualified compatibility with Pb−free board mount assembly processing. Existing packages that are currently offered solely with a Pb−free finish will also change part numbers. This is intended to clearly identify parts that are Pb−free and qualified for compatibility with Pb−free board mount assembly processing. The MPN (Manufacturer Part Number) bar code label on the reel, tube or rail, and the intermediate boxes will have the "Pb−free 2LI" logo printed on those labels compliant to JEDEC standard JESD97. Pb−free products may also be identified by unique product marking. Pb−free products are marked with a G suffix to the part number on the package. However, if the package is too small to include the additional G character, the Pb−free package will be marked with a micro dot.

Available Now			
Axial Lead Button	POWERMITE™	SO−8	SSOP
Case 77	POWERTAP™	SOD−123	SSOVP
ChipFET™	PSOP−2	SOD−323	Surge Special
D^2PAK 3, 5, 7	QFN 5x5, 5x6, 7x7, 8x8	SOD−523	Surmetic
D^2PAK Discrete	QFN 2x2.2, 3x3, 4x4	SOEIAJ 8/14/16/20	TO−218
DFN 1.6x1.6, 3x1, 3x3, 3.3x3.3, 4x1.6	SC−59	SOIC Narrow 7/8/14/16	TO−220 3/5/7
DPAK	SC−70 3/5	SOIC Wide 16/18/20/24	TO−247
FCDCA	SC−74	SOIC 16W EP	TO−264
LQFP 32/52	SC−75	SON 6 B/S	TO−3
LQFP 52/64 EP	SC−82AB	SOT−223	TO−92
Micro8™/10 IC	SC−82 Dual	SOT−23 3 Pin	Top Can
Micro8 FET	SC−88	SOT−23 5 Pin	TQFP 48 EP
Micro Leadless 3	SC−88A	SOT−23 6 Pin	TSOP−5
MOSORB™/MiniMOSORB™	SC−89	SOT−23−L	TSOP−6
PDIP 7/8/14/16/18/20/24N/24W	SIDAC 1 & 3 Amp	SOT−553	TSSOP 8/14/16/20/24/48

Available Now			
PLCC 20/28/44	SMA & SMA B/S	SOT−563	US8
SMB	SOT−723 PowerFLEX™	SMC	SOT−89
Planned			
FCBGA 16/49 SOIC 32W SPAK 5/7			
Not Planned			
BGA CLCC QSOP CDIP PLLP (PQFN) SOT−143			

Qualification Plan:

The qualification requirements for Pb−free external lead finish differ for surface−mount device (SMD) or through−hole devices (THD).

For the THDs the primary qualification requirement is to demonstrate forward compatibility with new Pb−free solder pastes (based on SnCuAg). The tests performed typically include:

- Solderability with SnCuAg solder
- Resistance to Solder Heat

For the SMDs reclassification of the moisture sensitivity level (MSL) at a peak reflow temperature of 260°C is required in addition to solderability validation. The MSL reclassification is performed on the largest die size that is used in the package. The tests performed typically include:

- Preconditioned Highly Accelerated Stress Testing (PC−HAST) − 96 hours minimum
- Preconditioned Autoclave (PC−AC) − 96 hours minimum
- Preconditioned Temperature Cycling (PC−TC) − 500 cycles minimum
- (Preconditioning is performed at the target MSL for 260 +5/−0°C)
- Solderability with SnCuAg solder
- Resistance to Solder Heat (RSH − Solder Immersion)

Backward Compatibility

Backward compatibility is the capability for our customers to take one of our Pb−free products, mount it on their PC board and reflow it using solder containing lead (Pb). ON Semiconductor has conducted reflow tests of Pb−free parts using leaded solder reflow temperatures and processes to simulate this condition. Tests have been conducted at 210 to 230°C and results show that there will not be solderability issues.

Please Note: This does not apply to BGA, bumped die or Flip−Chip devices. If the parts are Pb−free they need to use a Pb−free reflow process.

Points of Contact:

- Your Local ON Semiconductor Sales Representative
- ON Semiconductor Technical Information Center 1−800−282−9855 (US & Canada) or via web at **http://www.onsemi.com/tech−support**
- **http://www.onsemi.com/pb−free**

SOLDERRM

Section 2

Soldering / Mounting Techniques

Soldering Considerations for Surface Mount Packages

RECOMMENDED FOOTPRINTS FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.

POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain/collector pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating ambient temperature, T_A. Using the values provided on the data sheet, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device. For example, for a SOT−223 device, P_D is calculated as follows.

$$P_D = \frac{150°C - 25°C}{156°C/W} = 800 \text{ milliwatts}$$

The 156°C/W for the SOT−223 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 800 milliwatts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain/collector pad. By increasing the area of the drain/collector pad, the power dissipation can be increased. Although the power dissipation can almost be doubled with this method, area is taken up on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figures 1, 2 and 3.

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

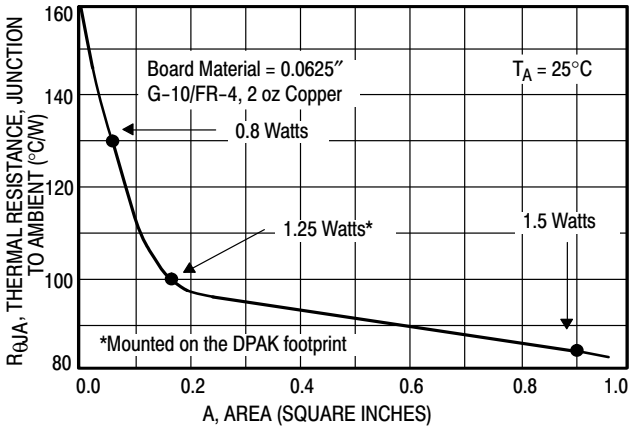


Figure 1. Thermal Resistance versus Drain Pad Area for the SOT−223 Package (Typical)

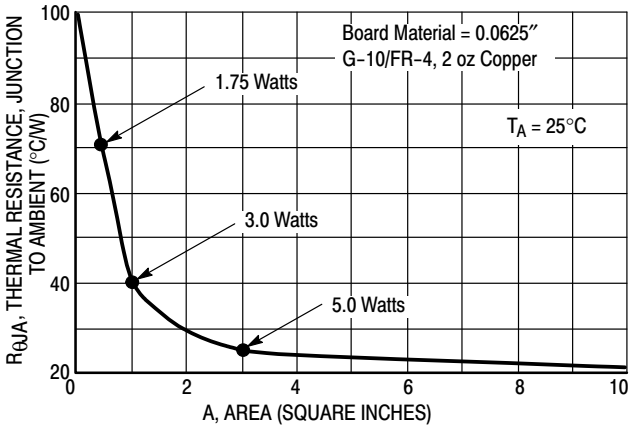


Figure 2. Thermal Resistance versus Drain Pad Area for the DPAK Package (Typical)

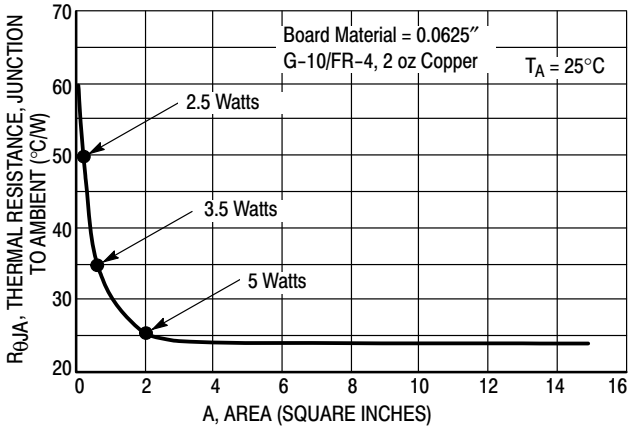


Figure 3. Thermal Resistance versus Drain Pad Area for the D²PAK Package (Typical)

SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC−59, SC−70/SOT−323, SOD−123, SOT−23, SOT−143, SOT−223, SO−8, SO−14, SO−16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and D^2PAK packages. If a 1:1 opening is used to screen solder onto the drain pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 4 shows a typical stencil for the DPAK and D^2PAK packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

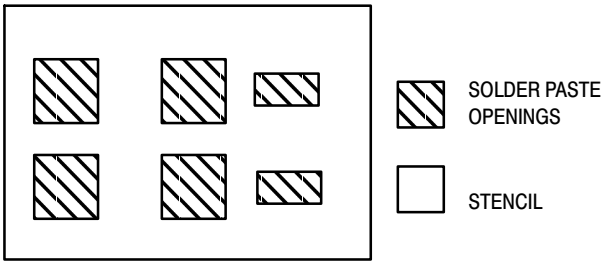


Figure 4. Typical Stencil for DPAK and D^2PAK Packages

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference should be a maximum of 10°C.
- The soldering temperature and time should not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used since the use of forced cooling will increase the temperature gradient and will result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the D^2PAK is not recommended for wave soldering.

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 5 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177−189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

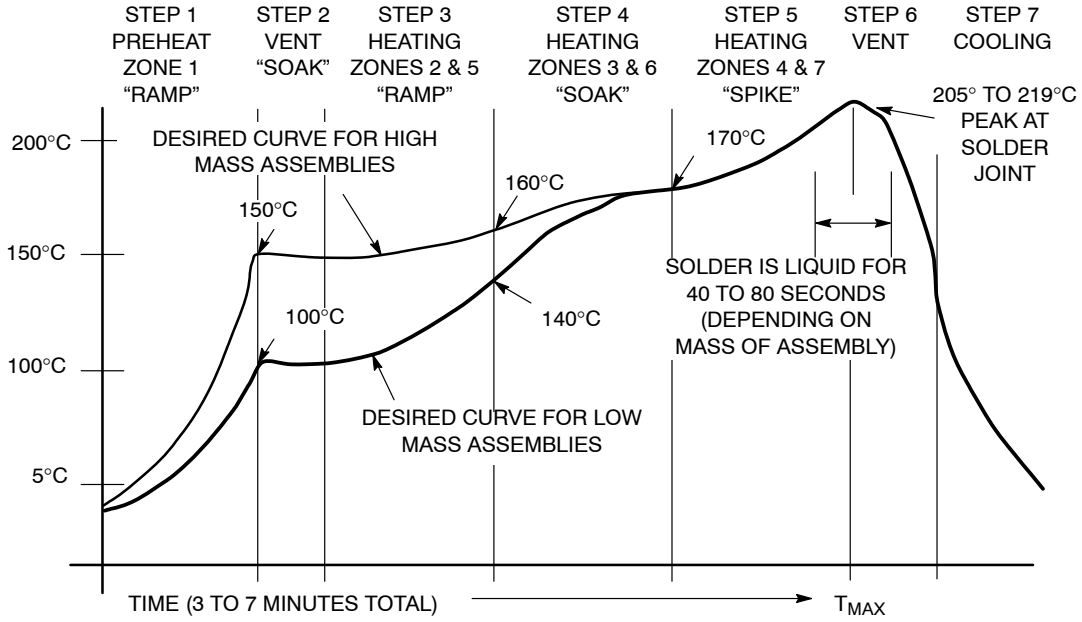


Figure 5. Typical Tin Lead (SnPb) Solder Heating Profile

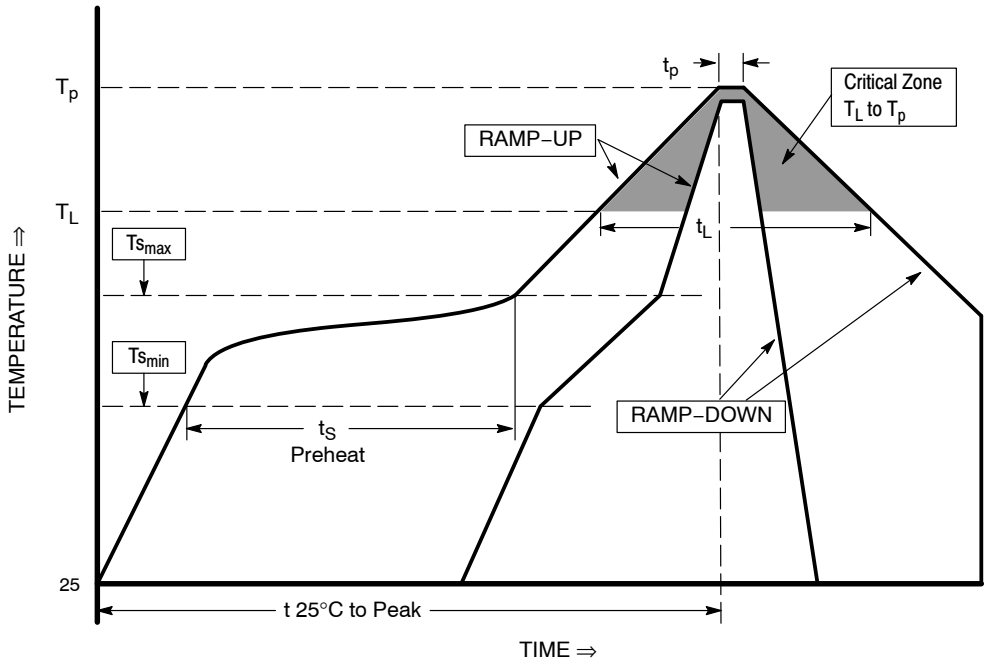
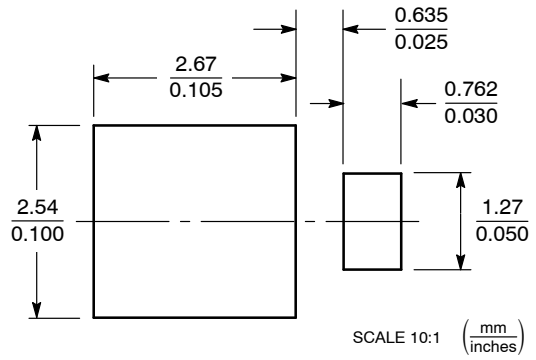


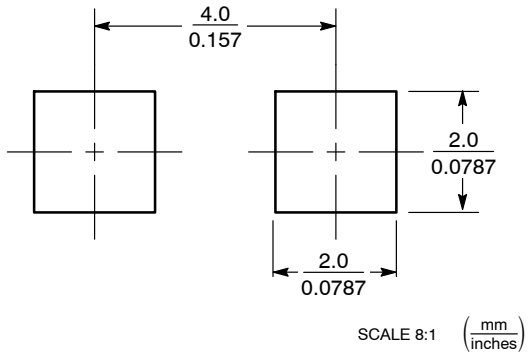
Figure 6. Typical Pb−Free Solder Heating Profile

Profile Feature	Pb−Free Assembly
Average Ramp−Up Rate (Ts_{max} to Tp)	3°C/second max
Preheat Temperature Min (Ts_{min}) Temperature Max (Ts_{max}) Time (ts_{min} to ts_{max})	 150°C 200°C 60−180 seconds
Time maintained above Temperature (T_T) Time (t_T)	 217°C 60−150 seconds
Peak Classification Temperature (Tp)	260°C +5/−0
Time within 5°C of actual Peak Temperature (tp)	20−40 seconds
Ramp−Down Rate	6°C/second max
Time 25°C to Peak Temperature	8 minutes max

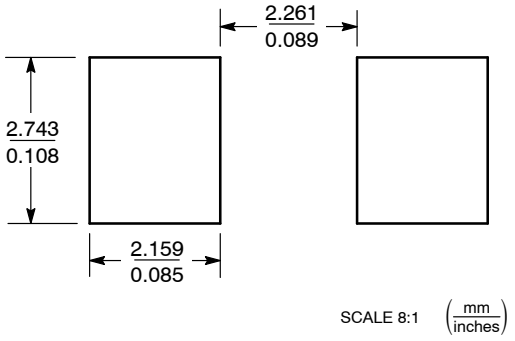
Footprints for Soldering



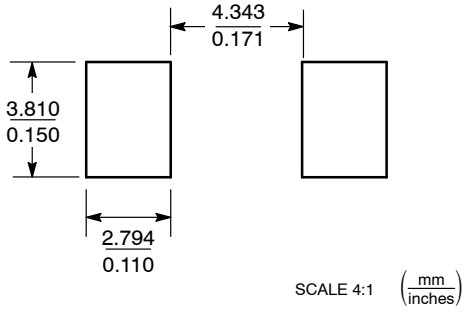
POWERMITE®



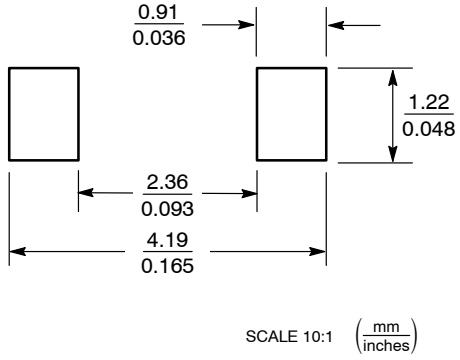
SMA



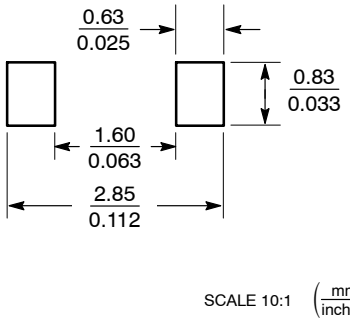
SMB



SMC

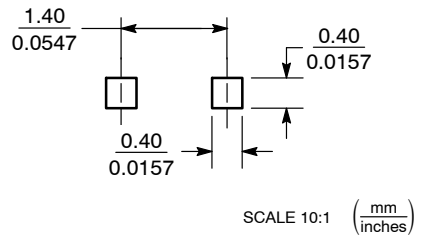


SOD−123



SOD−323

Footprints for Soldering (continued)



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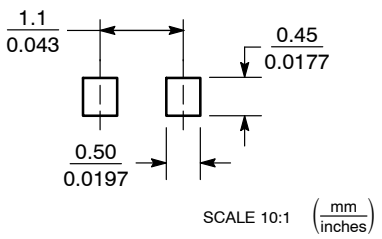
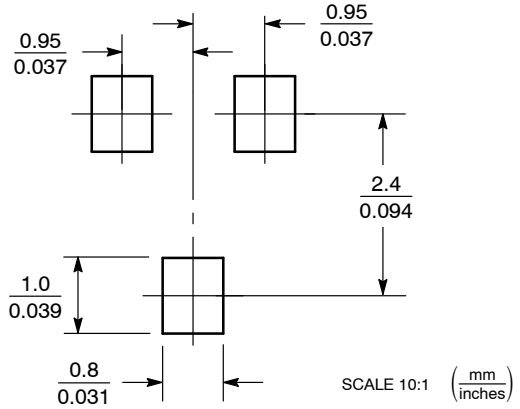
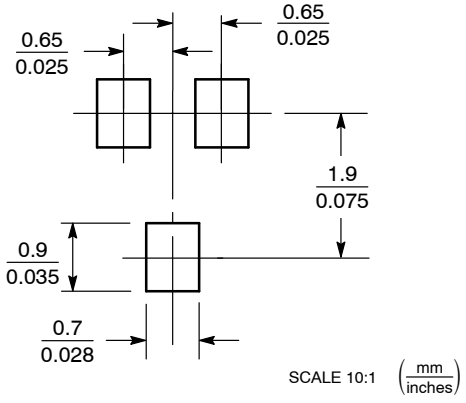


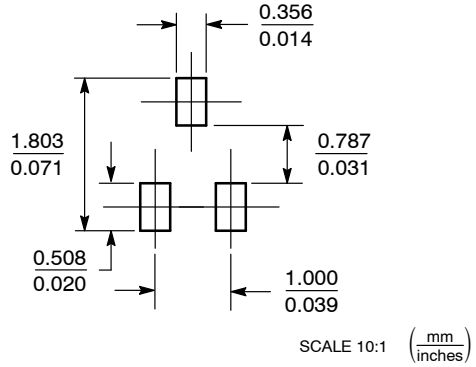
SOD−723



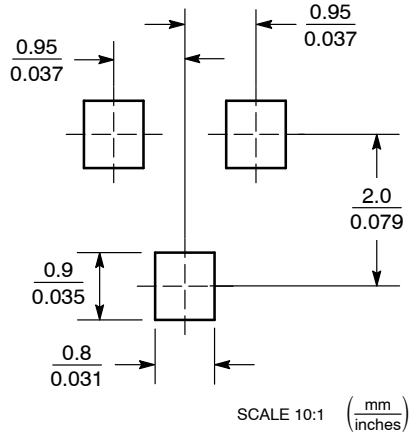
SC−59



SC−70/SOT−323



SC−75/SC−89/SOT−416



SOT−23

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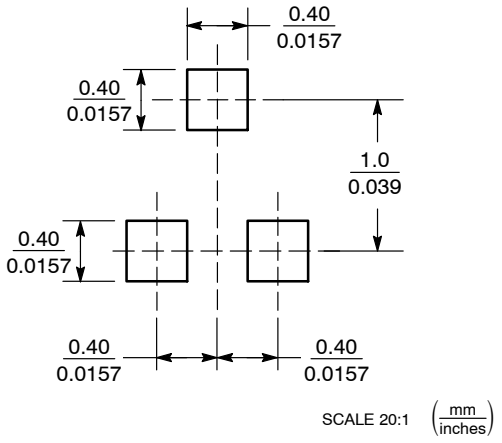

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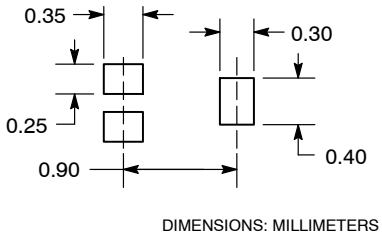

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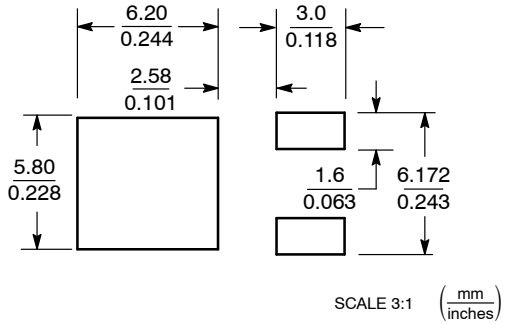
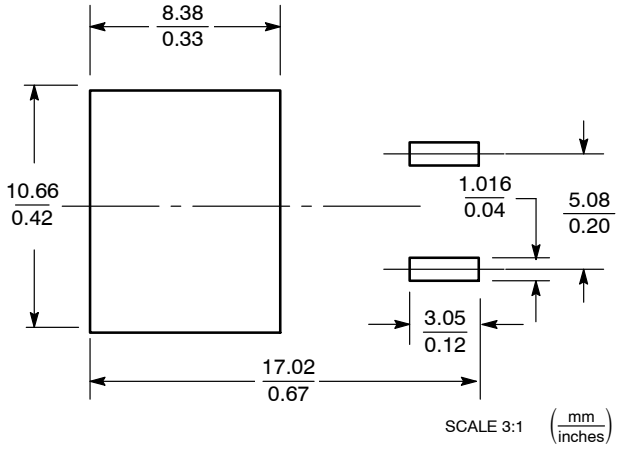
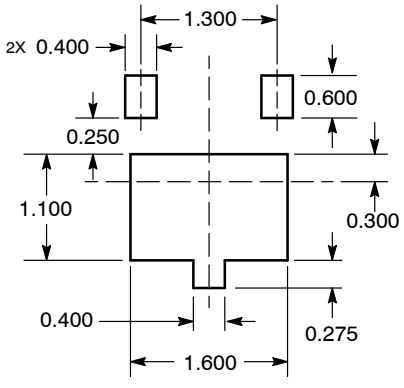


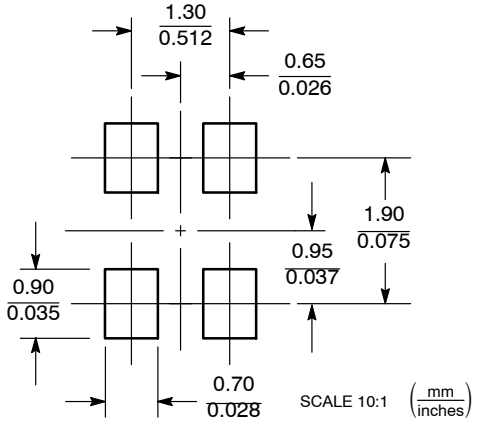
DPAK



D^{2}PAK

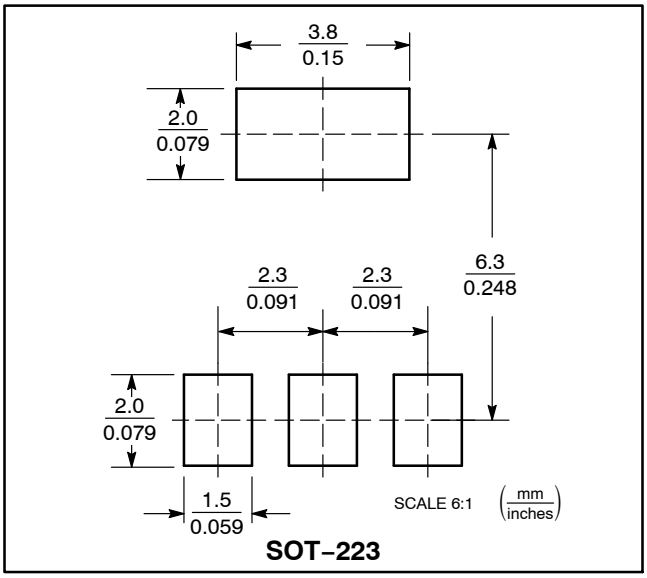


WDFN3



SC−82AB

Footprints for Soldering (continued)



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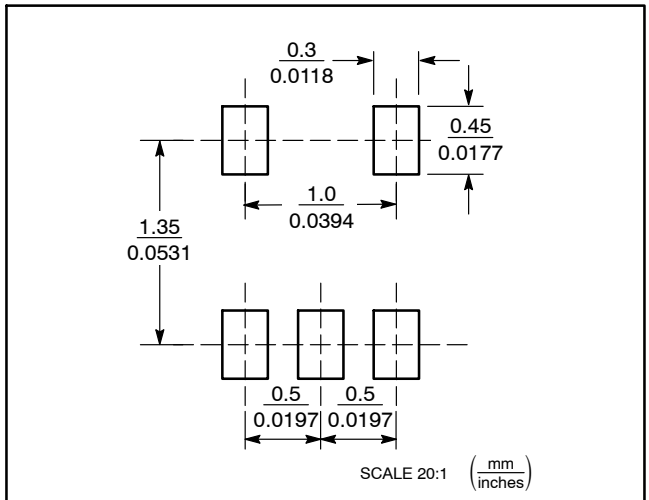

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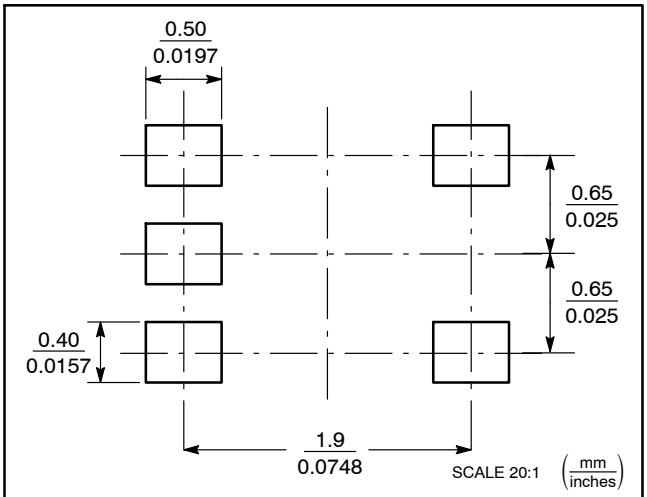

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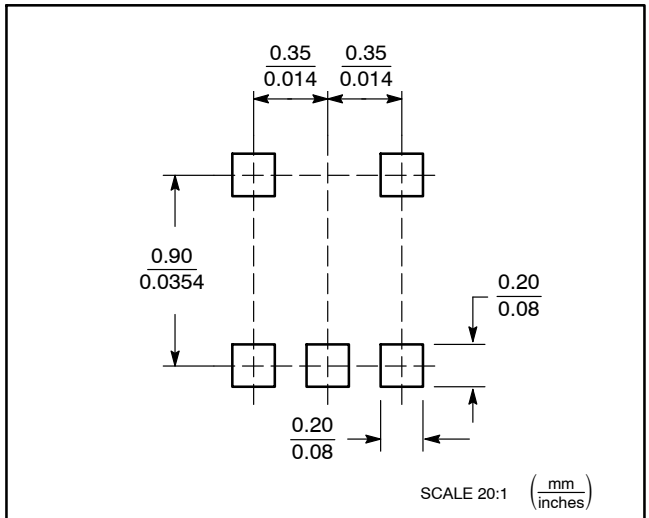

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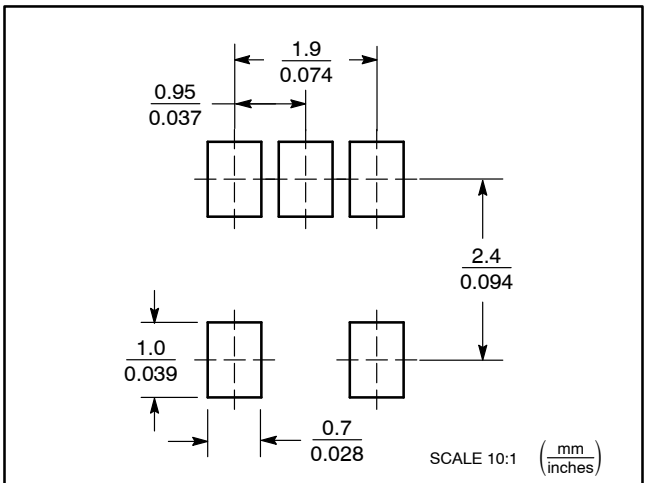
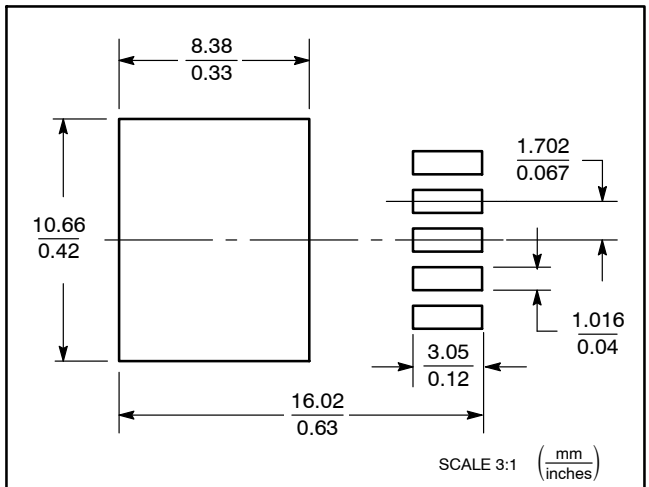
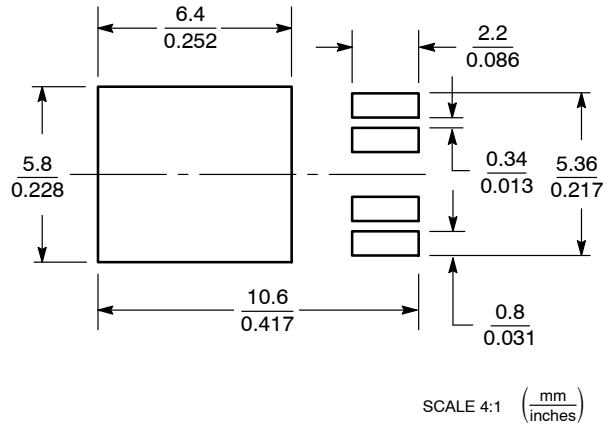


THIN SOT23−5/TSOP−5/SC59−5

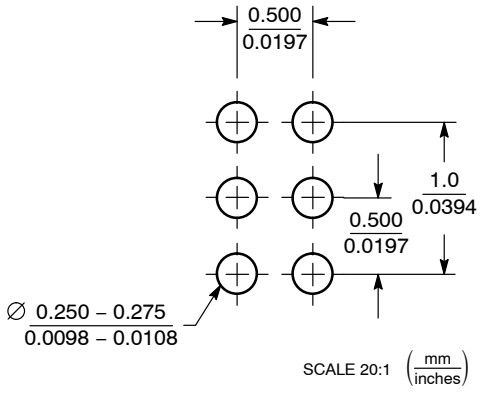


5−LEAD D²PAK

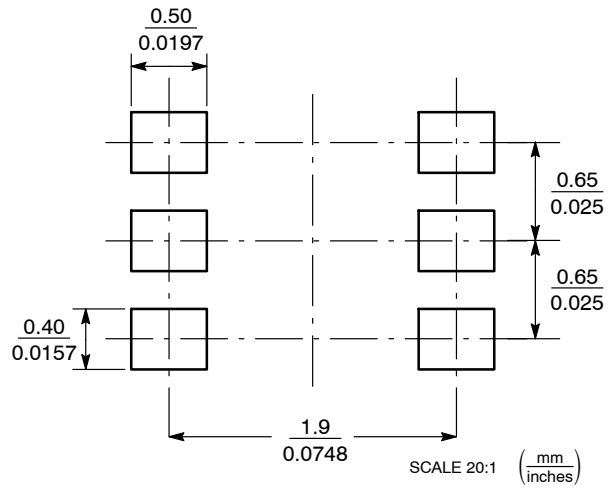
Footprints for Soldering (continued)



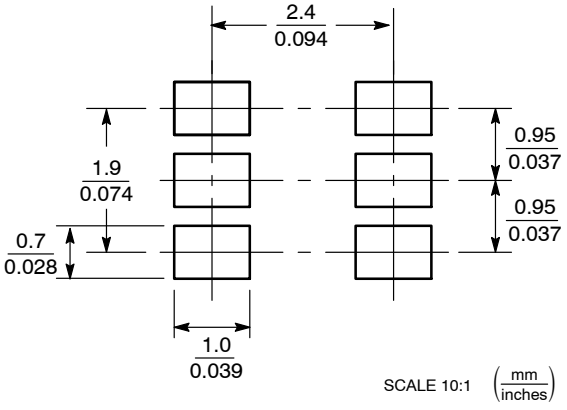
5−LEAD DPAK CENTRAL LEAD CROP



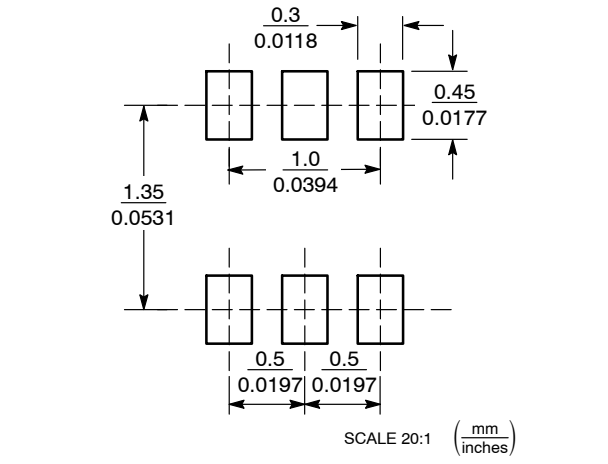
6 PIN FLIP−CHIP
(1.00 x 1.50 mm, 0.5 Pitch)



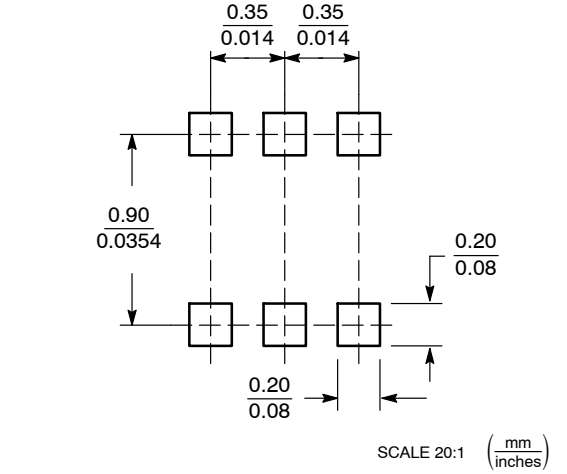
SC−88/SC70−6/SOT−363



SC−74/SC−74R

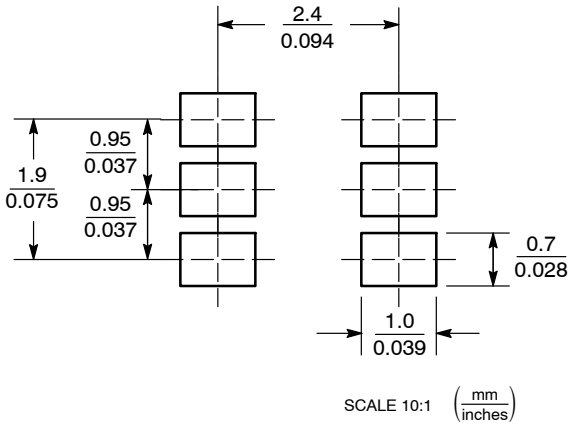


SOT−563

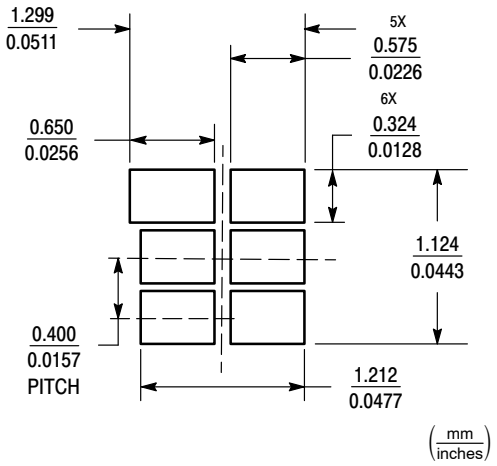


SOT−963

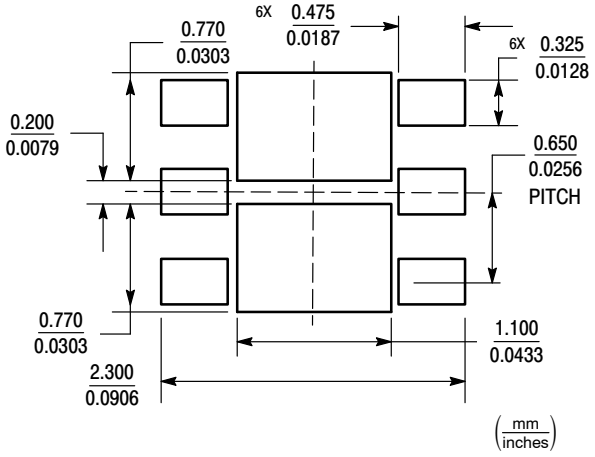
Footprints for Soldering (continued)



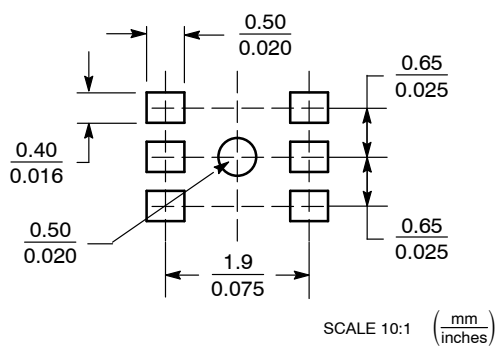
TSOP−6



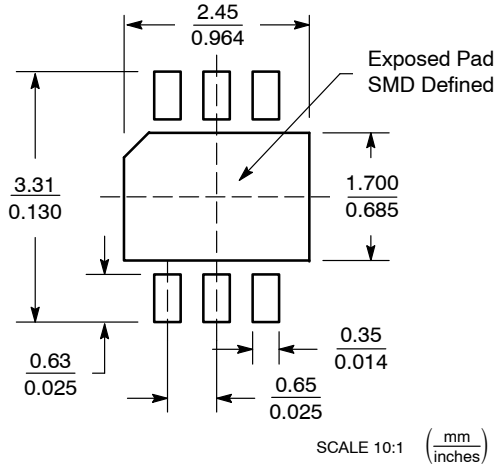
UDFN6/WDFN6, 1.2 x 1



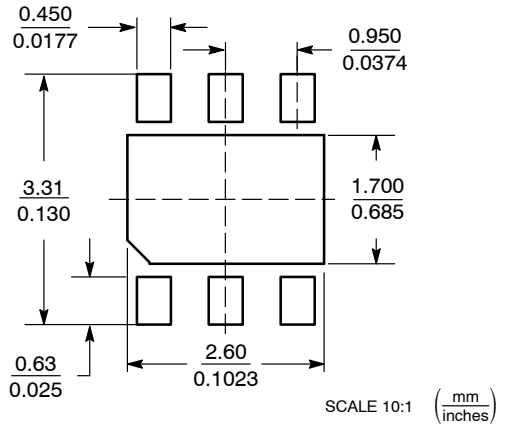
DFN6, 2 x 2



DFN6, 2 x 2.2

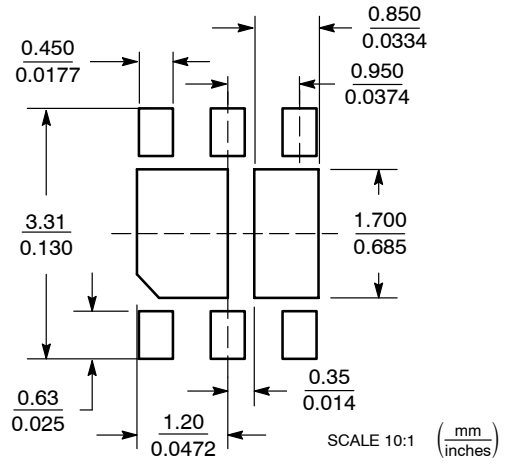


DFN6, 3 x 3, Single Flag

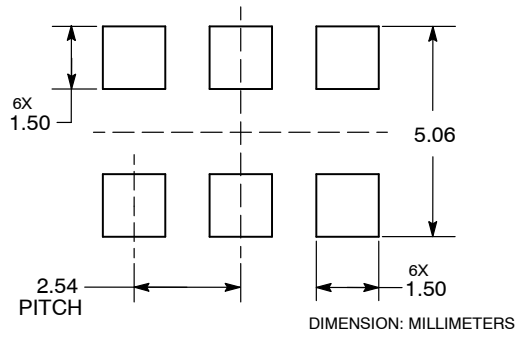


DFN6, 3 x 3, Single Flag

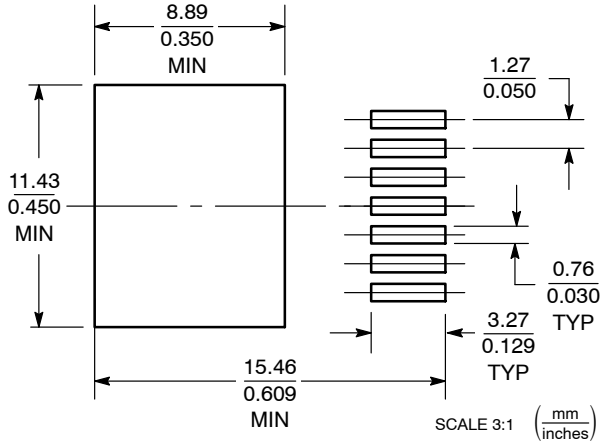
Footprints for Soldering (continued)



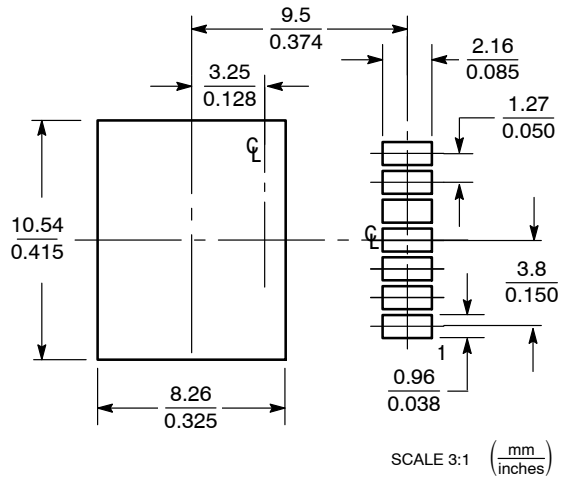
DFN6, 3 x 3, Dual Flag



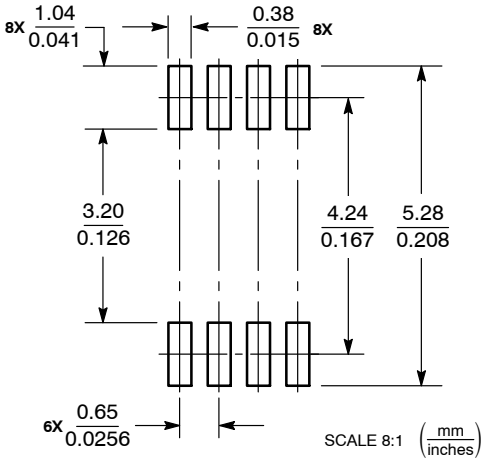
CLCC−6, 7 x 5 mm



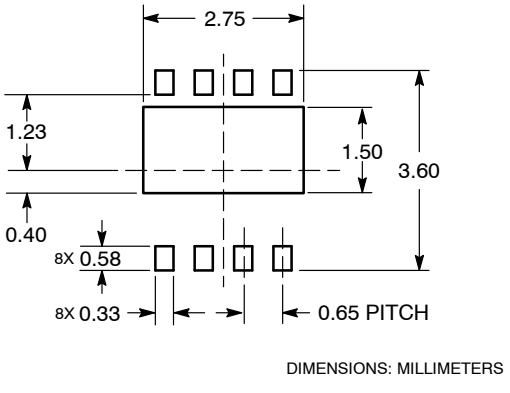
7−LEAD D²PAK



7−LEAD D²PAK, SHORT LEAD

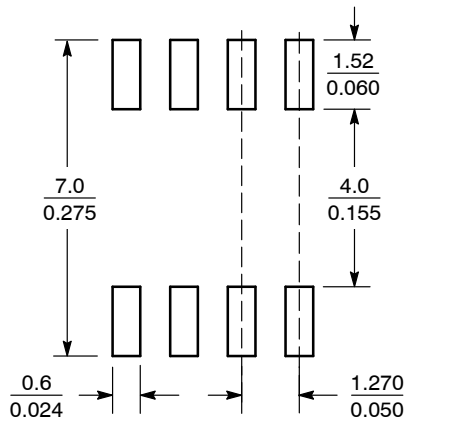


Micro8™

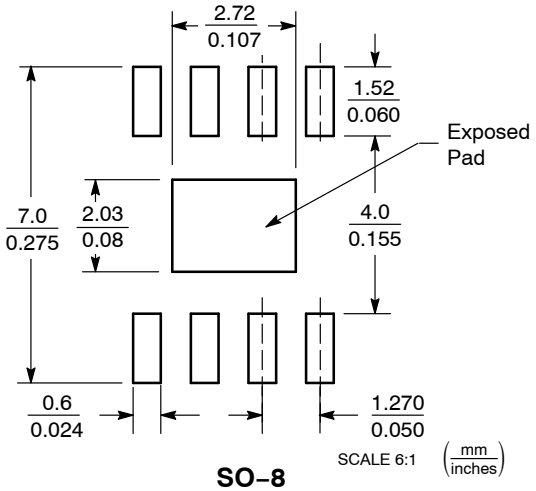


Micro8 Leadless

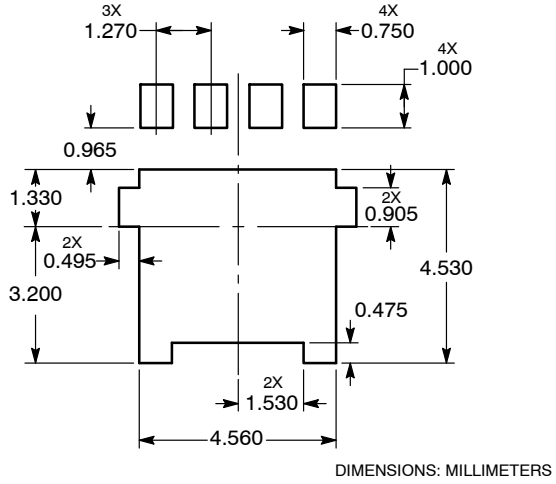
Footprints for Soldering (continued)



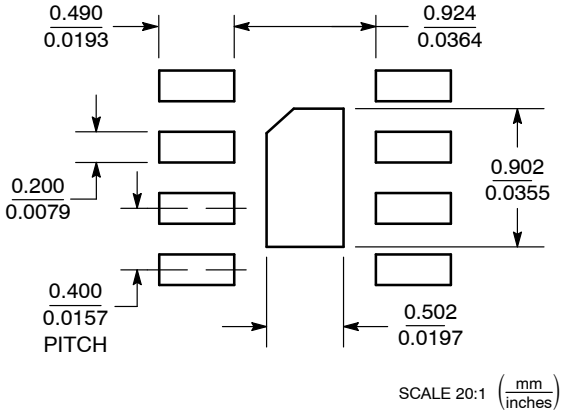
SO−8



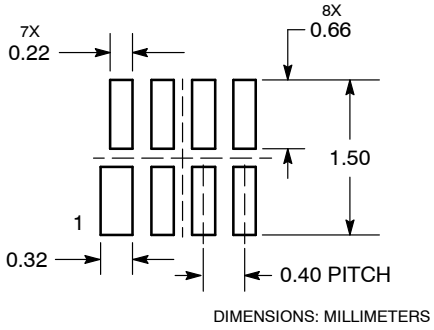
SO−8
Exposed Pad



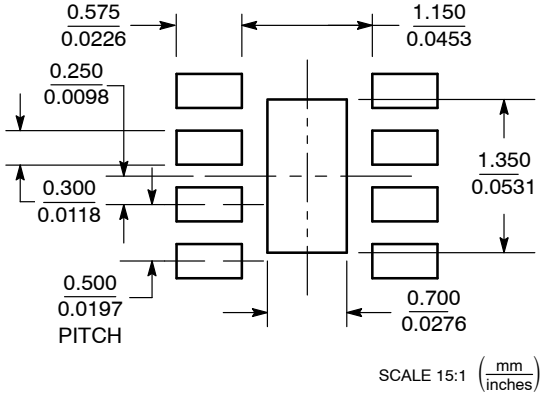
SO8FL (DFN6), 5 x 6



DFN8/UDFN8, 1.6 x 1.6

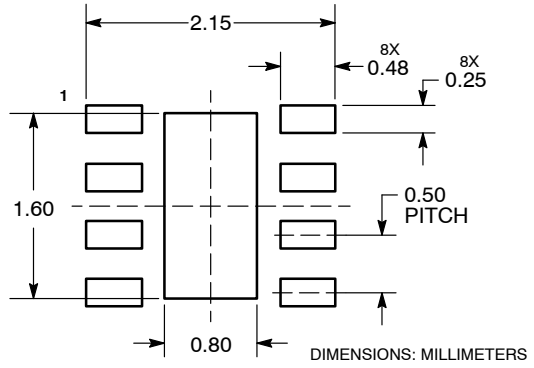


UDFN8, 1.8 x 1.2

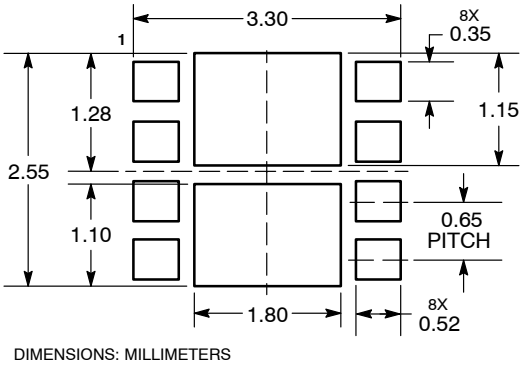


DFN8, 2 x 2

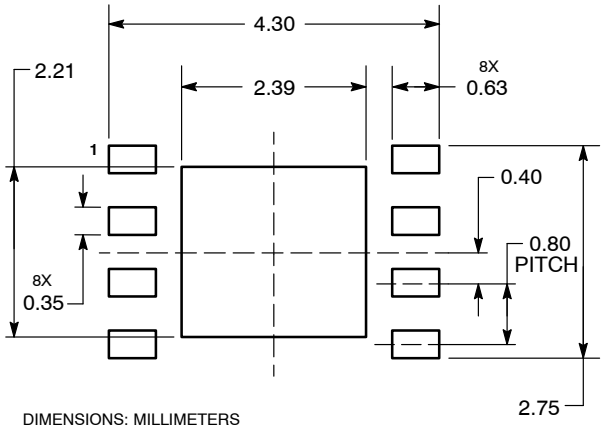
Footprints for Soldering (continued)



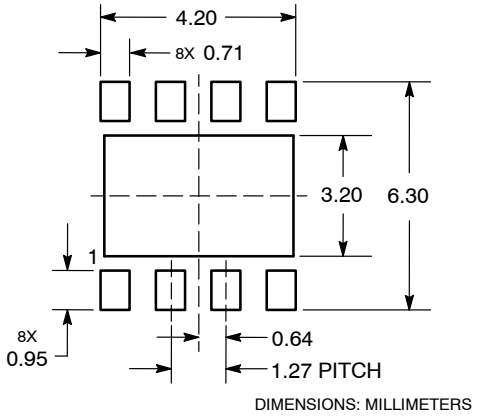
UDFN8, 2 x 2.2



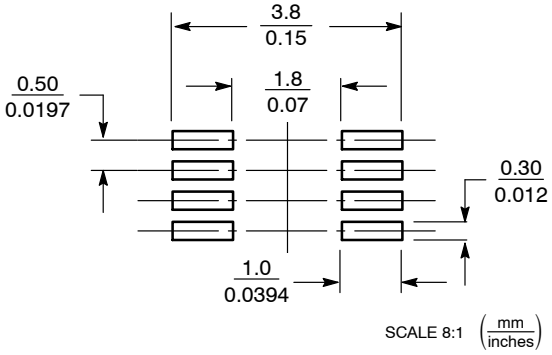
DFN8, 3 x 3



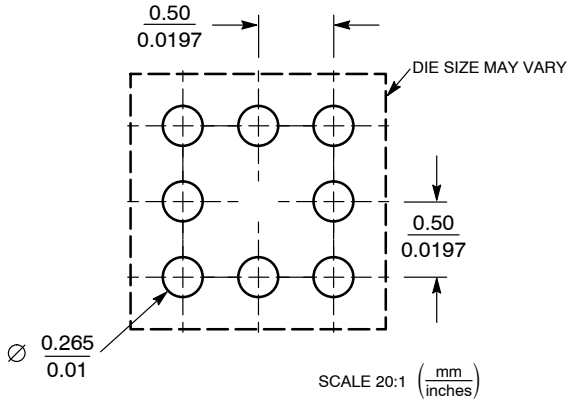
DFN8, 4 x 4



DFN8, 5 x 6

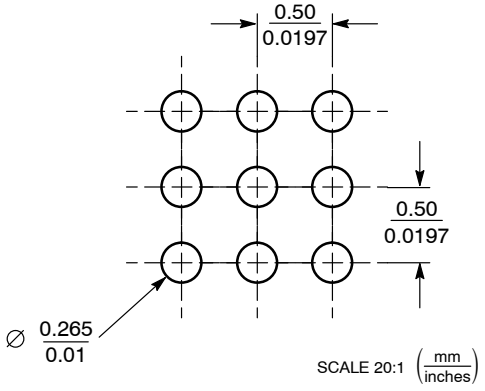


US8

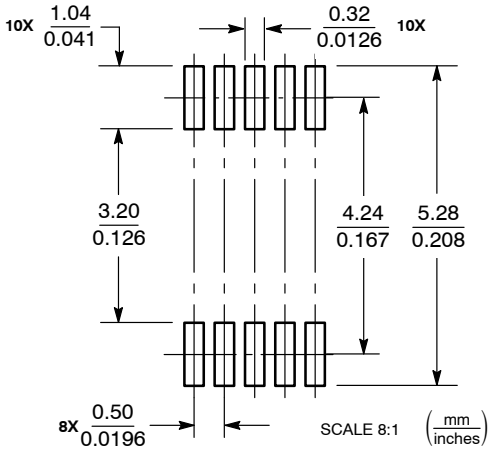


8−Bump
(Flip−Chip)

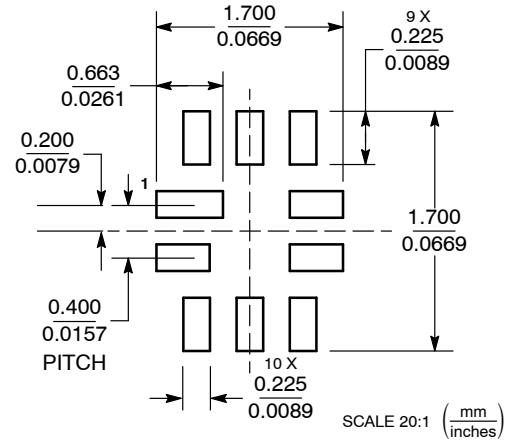
Footprints for Soldering (continued)



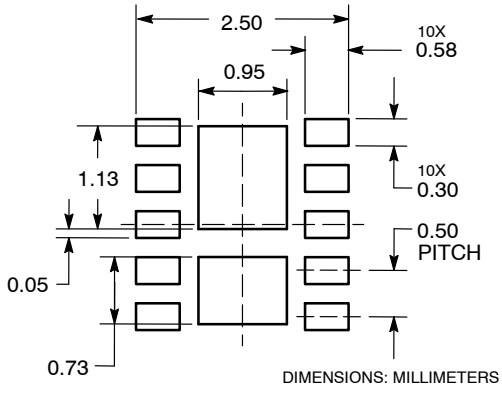
9−Bump
(1.550 x 1.550 mm)



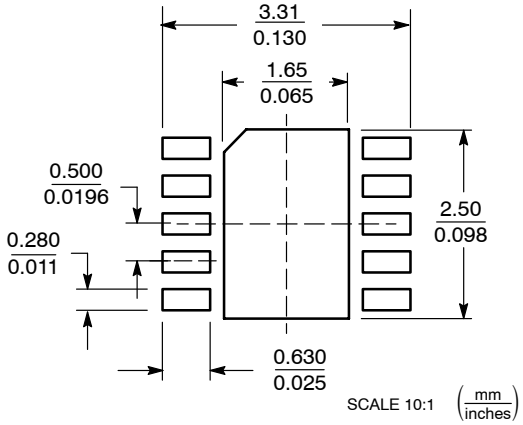
Micro10



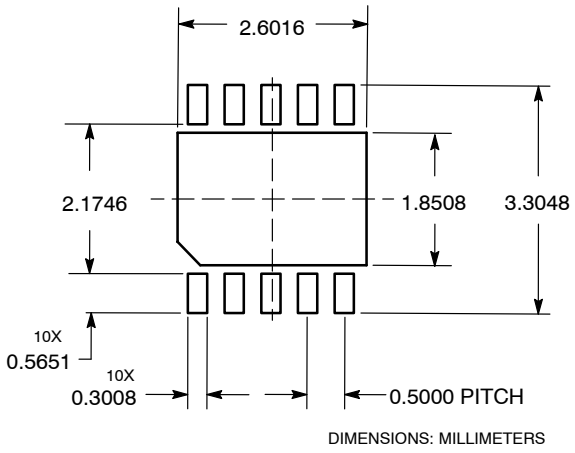
UQFN10/WQFN10, 1.4 x 1.8 mm



WDFN10, 2.5 x 2 mm

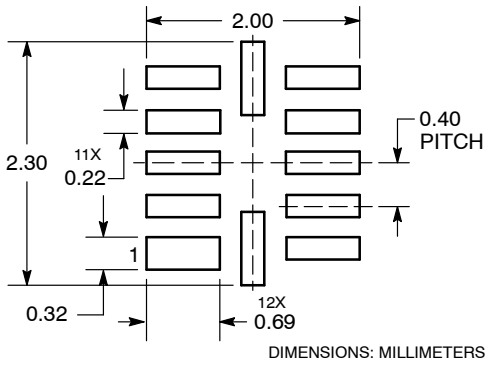


DFN10, 3 x 3 mm

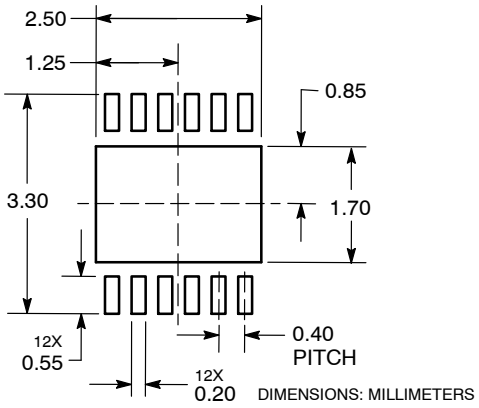


UDFN10

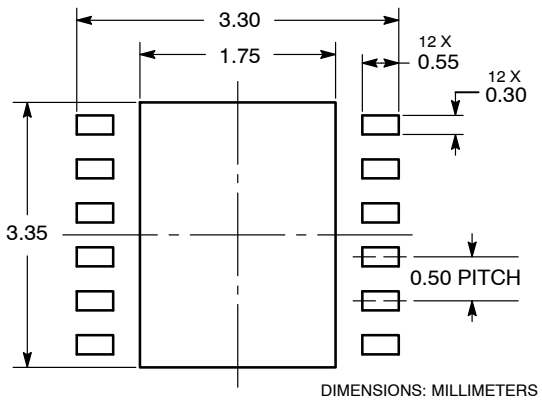
Footprints for Soldering (continued)



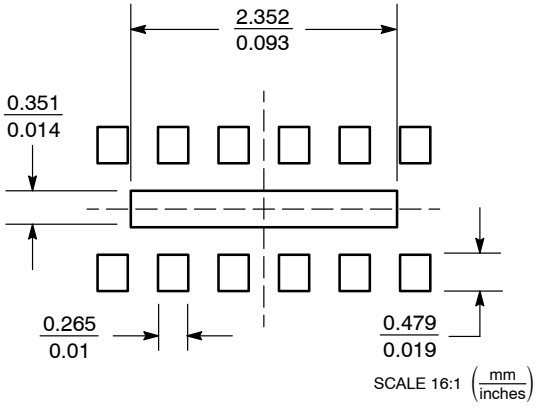
UQFN12, 1.7 x 2



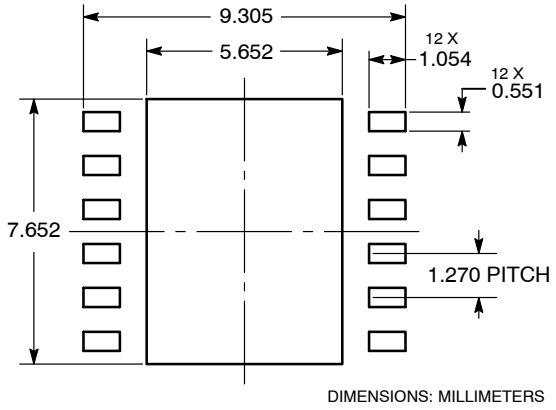
DFN12, 3 x 3



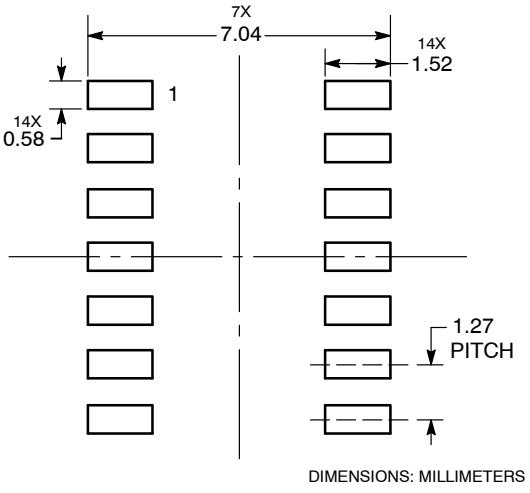
WDFN12, 3 x 4



DFN12

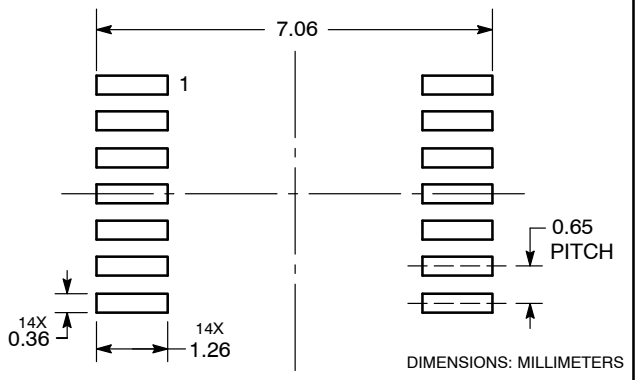


PLLP−12

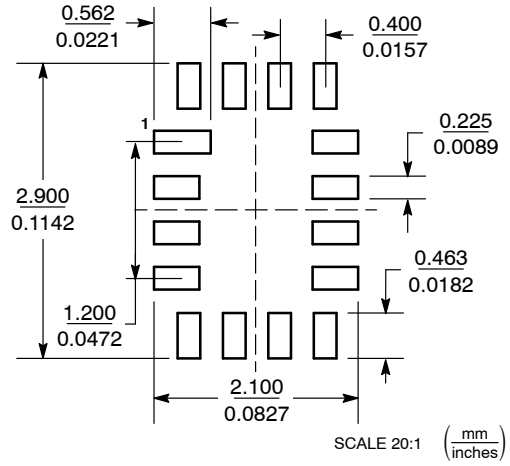


SOIC−14

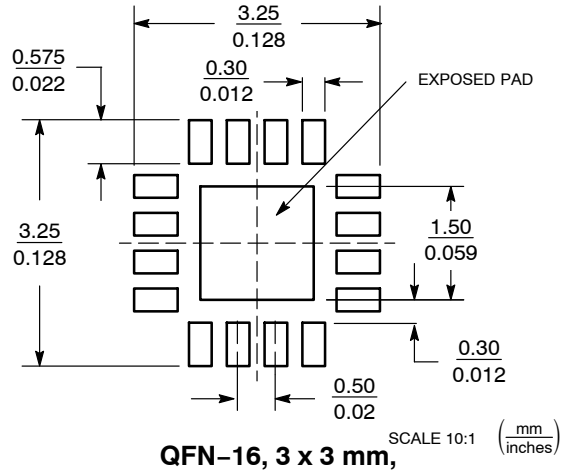
Footprints for Soldering (continued)



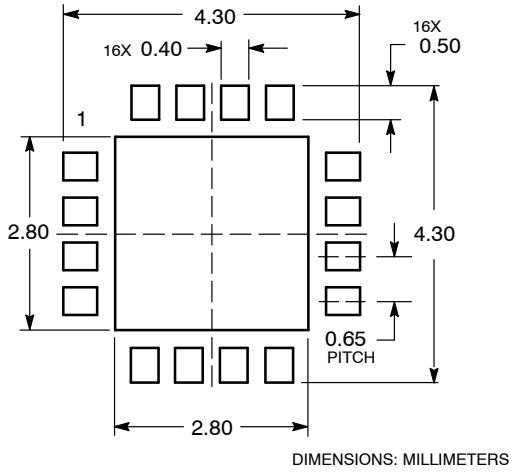
TSSOP−14



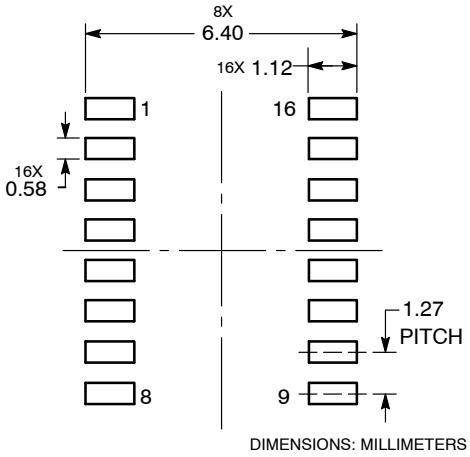
UQFN16/WQFN16, 1.8 x 2.6 mm



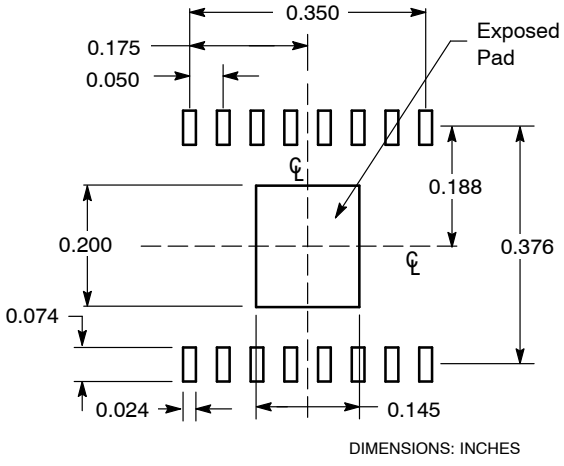
QFN−16, 3 x 3 mm, EP 2 x 2 mm



QFN16, 4 x 4 mm

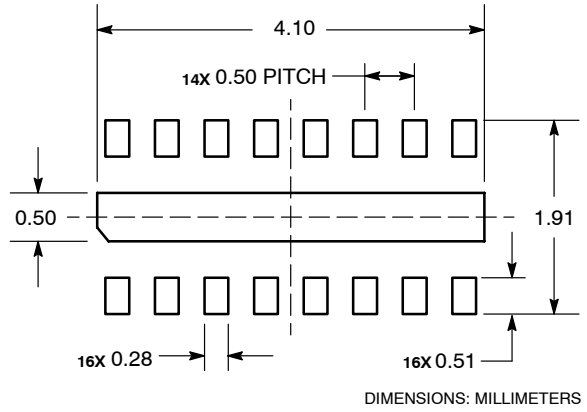


SOIC−16

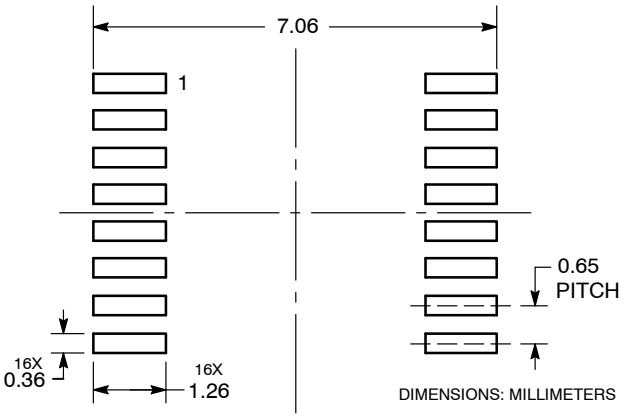


SOIC16−EP

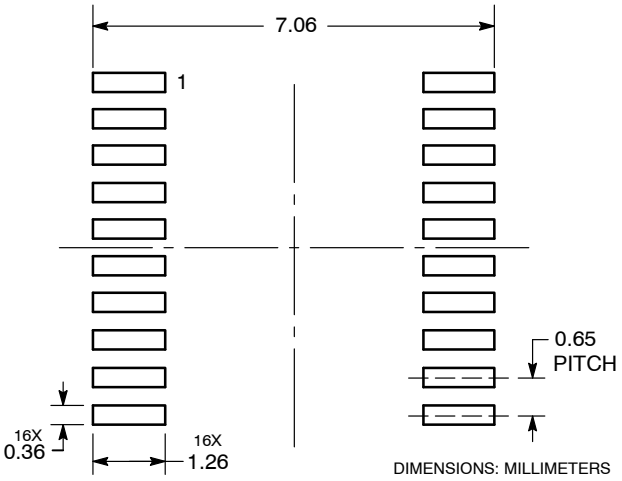
Footprints for Soldering (continued)



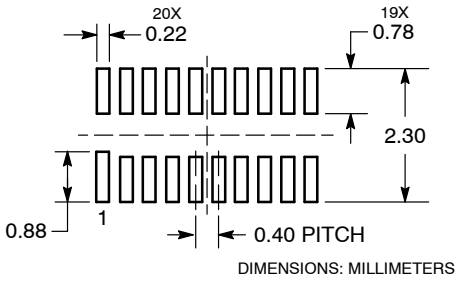
DFN16



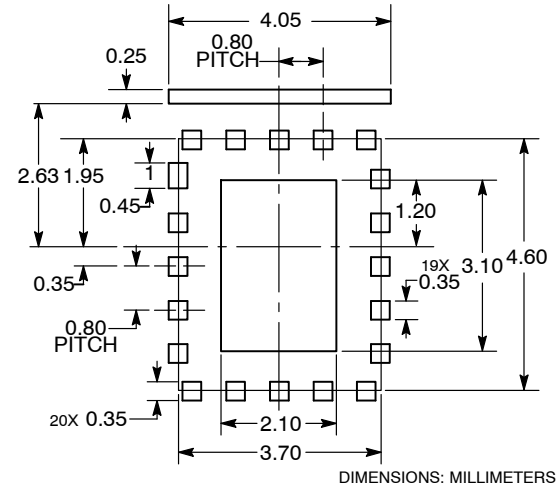
TSSOP−16



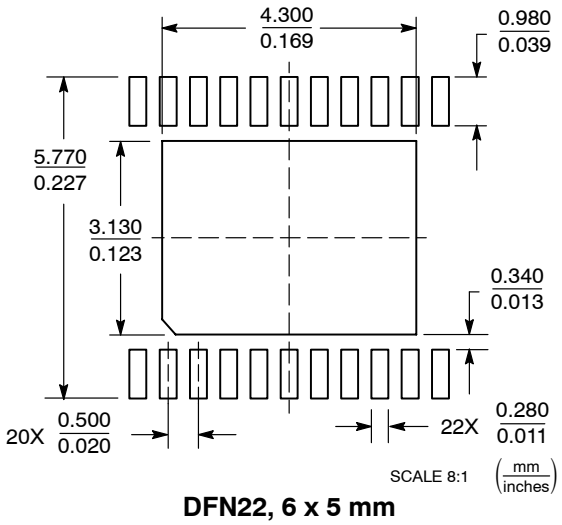
TSSOP−20



UDFN20, 4 x 2

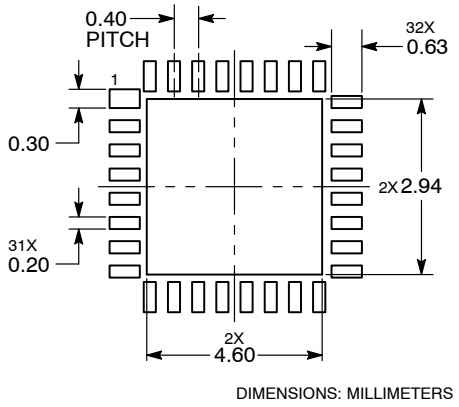


LLGA−20, 6 x 5

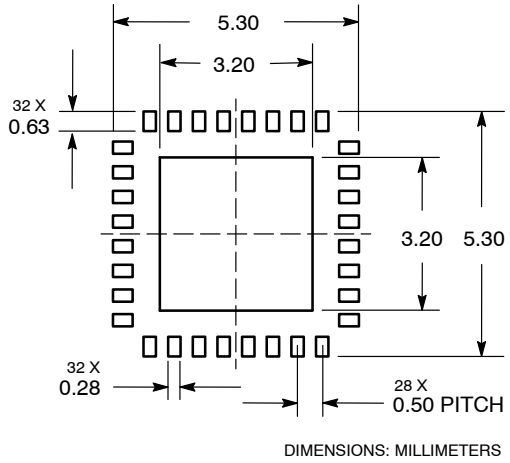


DFN22, 6 x 5 mm

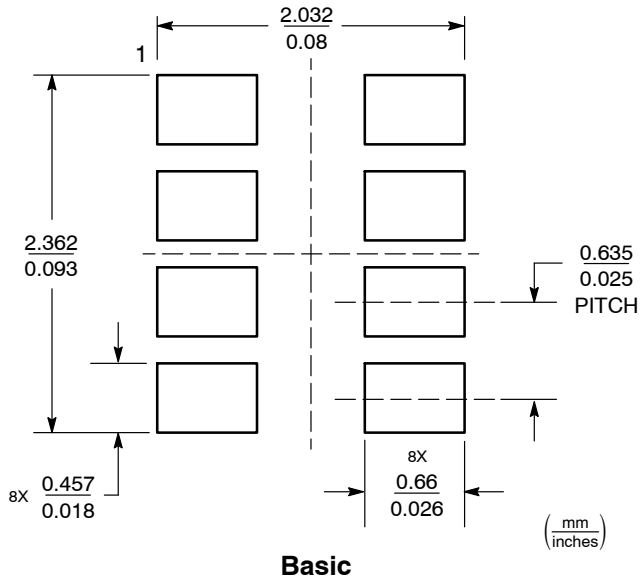
Footprints for Soldering (continued)



TLLGA32, 4 x 4



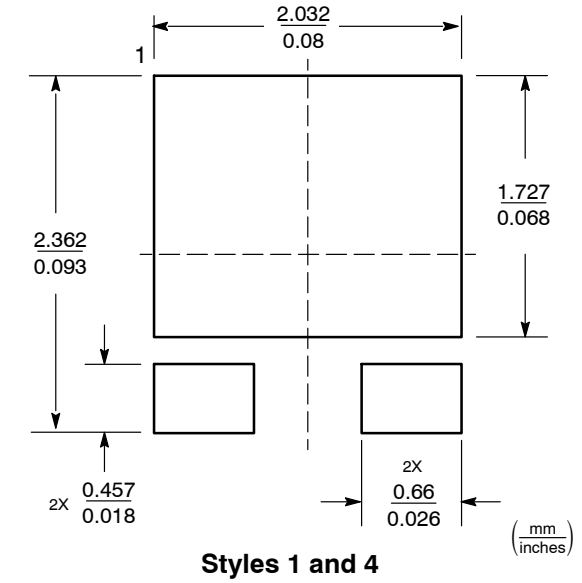
QFN32, 5 x 5 mm



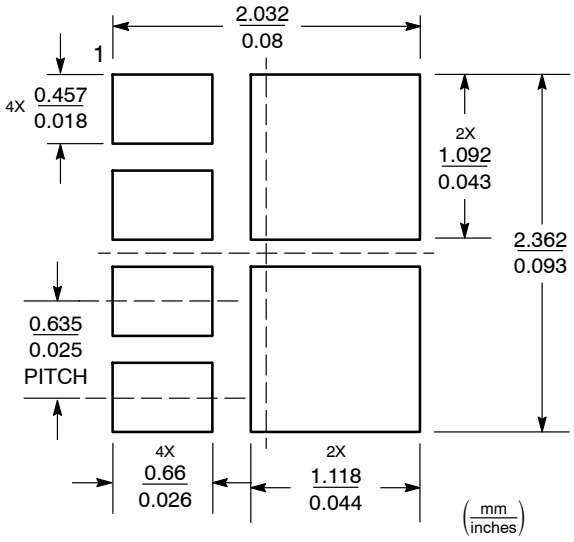
Basic

ChipFET

Footprints for Soldering (continued)



Styles 1 and 4



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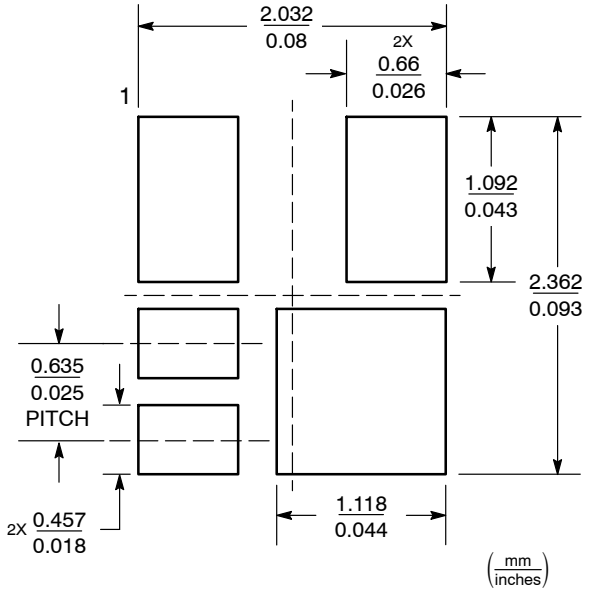

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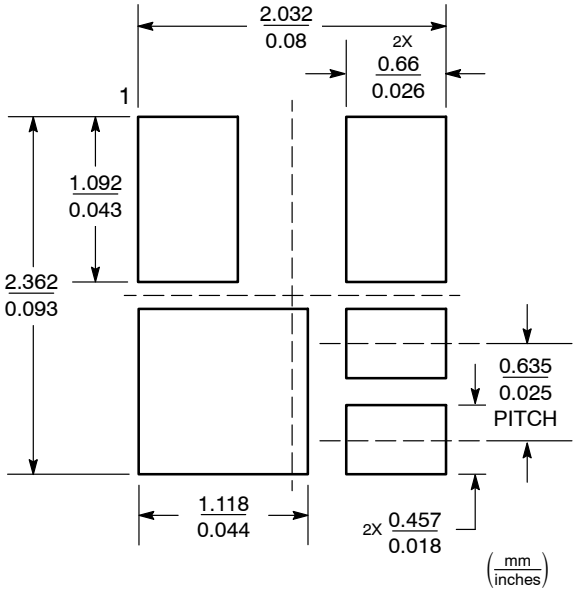

Style 5

ChipFET (continued)

AND8211/D

Board Level Application Notes for DFN and QFN Packages

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ON Semiconductor®

http://onsemi.com

APPLICATION NOTE

INTRODUCTION

Various ON Semiconductor components are packaged in an advanced Dual or Quad Flat−Pack No−Lead package (DFN/QFN). The DFN/QFN platform represents the latest in surface mount packaging technology, it is important that the design of the Mounting Pads of the Printed Circuit Board (PCB), Soldermask and Stencil pattern, along with the assembly process, all follow the suggested guidelines outlined in this document.

DFN/QFN Package Overview

The DFN/QFN platform offers a versatility which allows either a single or multiple semiconductor devices to be connected together within a leadless package. This packaging flexibility is illustrated in Figure 7 where four devices are packaged together with a custom pad configuration.

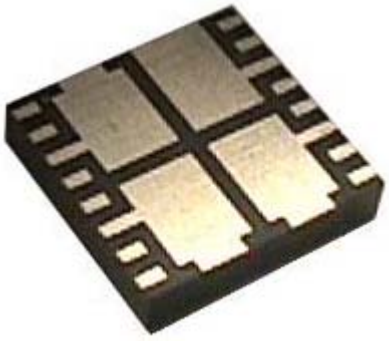


Figure 7. The Underside of a 4−Chip 16 Pin DFN Package

Figure 8 illustrates a single site DFN semiconductor device package which allows for a large device.

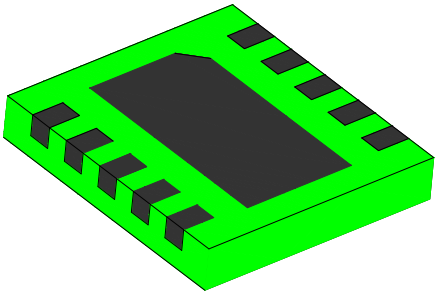


Figure 8. The Underside of a Single−Chip 10 Pin DFN Package

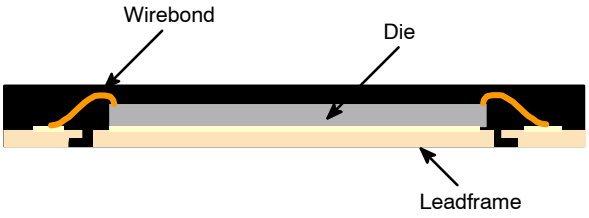


Figure 9. Cross−Section of a Single−Chip DFN Package

Figure 9 illustrates how the package height is reduced to a minimum by having both the die and wirebond pads on the same plane. When mounted, the leads are directly attached to the board without a space−consuming standoff, which is inherent in a leaded package.

Figure 9 also illustrates how the ends of the leads are flush with the edge of the package. This configuration allows for the maximum die size within a given footprint, while maximizing the board space efficiency.

In addition to these features, the DFN/QFN package has excellent thermal dissipation and reduced electrical parasitics due to its efficient and compact design.

Printed Circuit Board Solder Pad Design Guidelines

Refer to the case outline (specification sheet) drawing for the specific DFN/QFN package to be mounted. Based on the nominal package footprint dimensions from the case drawing. The PCB mounting pads need to be larger than the nominal package footprint (see Figure 10).

Note: On the occasion that there is not enough room to grow the PCB mounting pads per these guidelines, the recommendation would be to come as close to these guidelines as possible.

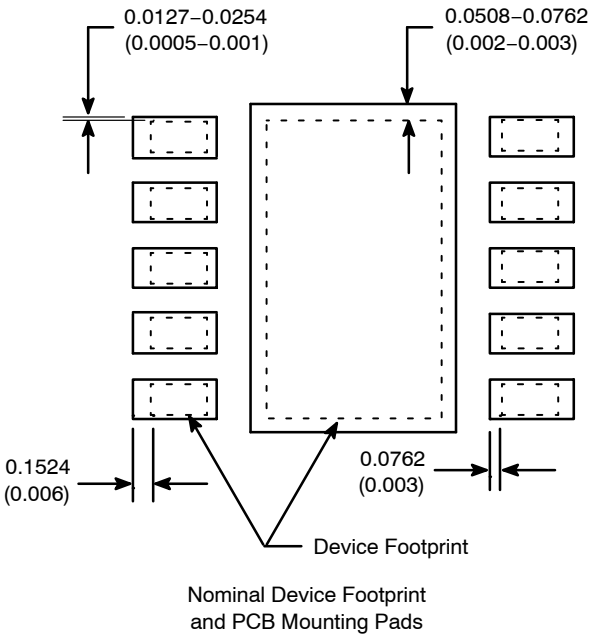


Figure 10. 10 Pin DFN Package Footprint Shown with PCB Mounting Pads

Printed Circuit Board Solder Mask Design Guidelines

SMD and NSMD Pad Configurations

There are two different types of PCB pad configurations commonly used for surface mount leadless DFN/QFN style packages. The different configurations are:

1. Non Solder Masked Defined (NSMD)
2. Solder Masked Defined (SMD)

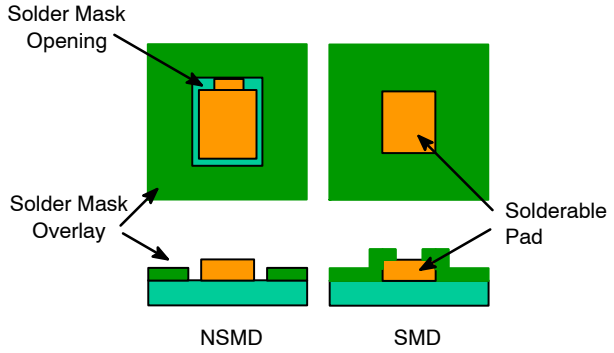


Figure 11. Comparison of NSMD vs. SMD Pads

As their titles describe, the NSMD contact pads have the solder mask pulled away from the solderable metallization, while the SMD pads have the solder mask over the edge of the metallization, as shown in Figure 11. With the SMD Pads, the solder mask restricts the flow of solder paste on the top of the metallization which prevents the solder from flowing along the side of the metal pad. This is different from the NSMD configuration where the solder will flow around both the top and the sides of the metallization.

Typically, the NSMD pads are preferred over the SMD configuration since defining the location and size of the copper pad is easier to control than the solder mask. This is based on the fact that the copper etching process is capable of a tighter tolerance than the solder masking process. This also allows for visual inspection of solder fillet.

In addition, the SMD pads will inherently create a stress concentration point where the solder wets to the pad on top of the lead. This stress concentration point is reduced when the solder is allowed to flow down the sides of the leads in the NSMD configuration.

Printed Circuit Board Solder Mask Design Guidelines

When dimensionally possible, the solder mask should be located within a range of 0.0762–0.1270 mm (0.003–0.005 in) away from the edge of the PCB mounting pad (see Figure 12). This spacing is used to compensate for the registration tolerances of the solder mask, as well as to insure that the solder is not inhibited by the mask as it reflows along the sides of the metal pad.

The solder mask web (between openings) is the controlling factor in the pattern, and needs to be held to a minimum of 0.1016 mm (0.004 in). This minimum is the current PCB suppliers standard minimum web for manufacturability. Because of this web restriction, solder mask openings around PCB pads may need to be less than the recommended shown. Whenever possible, keeping to the range given will provide for the best results.

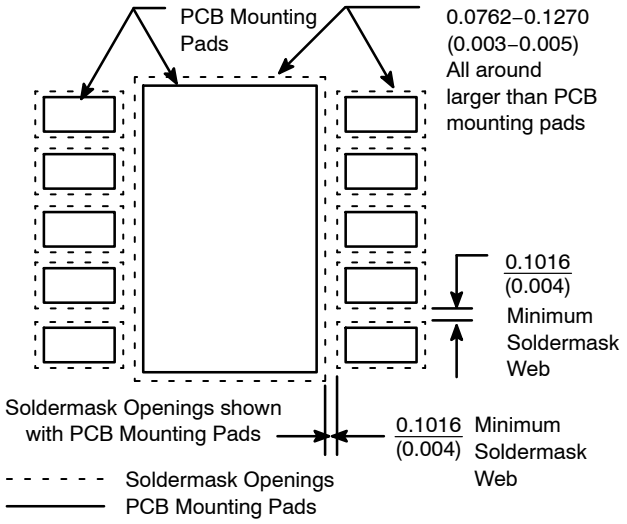


Figure 12. Typical DFN Package – PCB Mounting Pads Shown with Soldermask Openings

DFN/QFN Board Mounting Process

The DFN/QFN board mounting process is optimized by first defining and controlling the following.

1. Solderable metallization on the PCB contacts.
2. Choice of proper solder paste.
3. Solder paste on the PCB.
4. Package placement.
5. Reflow of the solder paste.
6. Final solder joint inspection.

Recommendations for each of these processes are located below.

PCB Solderable Metallization

There are currently three common solderable coatings which are used for PCB surface mount devices. In any case, it is imperative that the coating is uniform, conforming, and free of impurities to insure a consistant solderable system.

The first coating consists of an Organic Solderability Protectant (OSP) applied over the bare copper feature. OSP coating assists in reducing oxidation in order to preserve the copper metallization for soldering. It allows for multiple passes through reflow ovens without degradation of the solderability. The OSP coating is dissolved by the flux when the solder paste is applied to the metal features. Coating thickness recommended by OSP manufacturers is between 0.25 and 0.35 microns.

The second coating is a metalized coating which consists of plated electroless nickel over the copper pad, followed by a coat of immersion gold. The thickness of the electroless nickel layer is determined by the allowable internal material stresses and the temperature excursions the board will be subjected to throughout its lifetime. Even though the gold metallization is typically a self−limiting process, the thickness should be at least 0.05 μm thick, and not consist of more than 5% of the overall solder volume. Having excessive gold in the solder joint can create gold embitterment which may affect the reliability of the joint.

The third is a tin−lead coating, commonly called Hot Air Solder Level (HASL).This type of PCB pad finish is not recommended for DFN/QFN type packages. The major issue is the inability to consistently control the amount of solder coating applied to each pad. This results in dome−shaped pads of various heights. As the industry drives for finer and finer pitch, solder bridging becomes a common problem between mounting pads.

Solder Type

Solder paste such as Cookson Electronics' WS3060 with a Type 3 or smaller sphere size is recommended. The WS3060 has a water−soluble flux for cleaning. Cookson Electronics' PNC0106A can be used if a no−clean flux is preferred.

Solder Screening onto the PCB

Stencil screening the solder paste onto the PCB is commonly used in the industry. The recommended stencil thickness used is 0.075 mm to 0.127 mm (0.003 in to 0.005 in). The sidewalls of the stencil openings should be tapered approximately 5° to facilitate the release of the paste when the stencil is removed from the PCB.

The stencil opening should be the same size as the PCB mounting pad. The exception is when there is a large center flag on the device. Then the stencil opening should allow for 70−80% coverage of the PCB mounting pad. This opening should also be divided into smaller cavities to aid in the flow of solder during the reflow process (see Figure 13). Dividing the larger die pads into smaller screen openings reduces the risk of solder voiding and allows the solder joints for the smaller terminal pads to be at the same height as the larger ones.

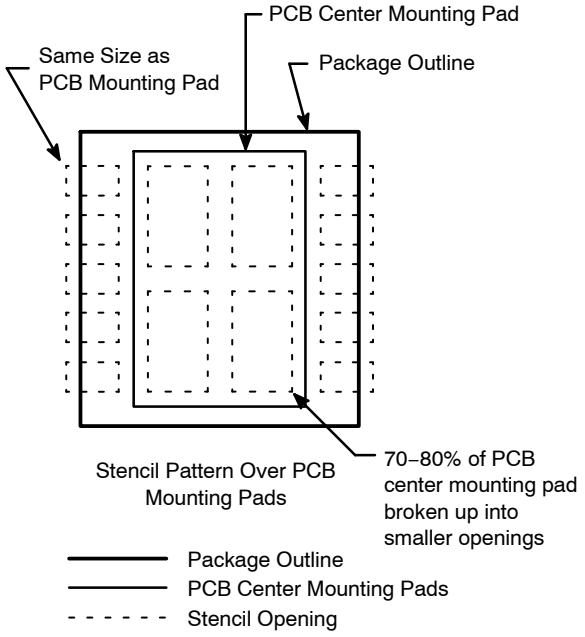


Figure 13. Typical DFN Package with Stencil Openings Shown Over PCB Mounting Pads

Package Placement onto the PCB

Pick and place equipment with the standard tolerance of ±0.05 mm (0.002 in) or better is recommended. The package will tend to center itself and correct for slight placement errors during the reflow process due to the surface tension of the solder.

Solder Reflow

Once the package is placed on the PC board along with the solder paste, a standard surface mount reflow process can be used to mount the part. Figures 14 and 15 are examples of standard reflow profiles for standard eutectic and lead free solder alloys.

The exact profile will be determined, and is available, by the manufacture of the paste since the chemistry and viscosity of the flux matrix will vary. These variations will require small changes in the profile in order to achieve an optimized process.

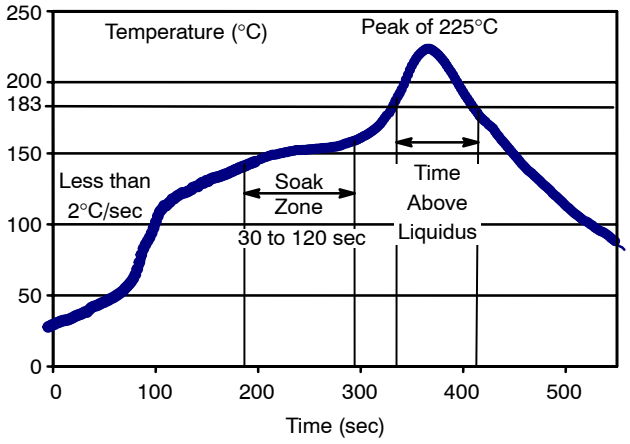


Figure 14. Typical Reflow Profile for Eutectic Tin/Lead Solder

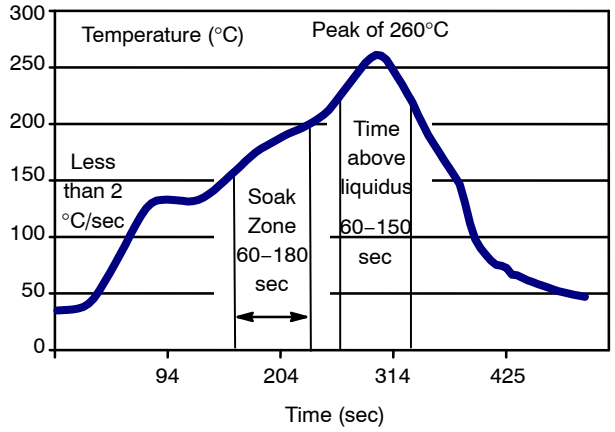


Figure 15. Typical Reflow Profile for Pb−Free Solder

In general, the temperature of the part should be raised not more than 2°C/sec during the initial stages of the reflow profile. The soak zone then occurs when the part is approximately 150°C and should last for 60 to 180 seconds for Pb−free profiles (30−120 sec for Eutectic profiles). Typically, extending the time in the soak zone will reduce the risk of voiding within the solder. The temperature is then raised and will be above the liquidus of the solder for 60 to 150 seconds for Pb−free profiles (30−100 sec for Eutectic profiles) depending on the mass of the board. The peak temperature of the profile should be between 245 and 260°C for Pb−free solder alloys (205−225°C) for eutectic solders.

If required, removal of the residual solder flux can be completed by using the recommended procedures set forth by the flux manufacturer.

Final Solder Inspection

The inspection of the solder joints is commonly performed with the use of an X−ray inspection system. With this tool, one can locate defects such as shorts between pads, open contacts, voids within the solder as well as any extraneous solder.

In addition to searching for defects, the mounted device should be rotated on its side to inspect the sides of the solder joints with an X−ray inspection system. The solder joints should have enough solder volume with the proper stand−off height so that an “Hour Glass” shaped connection is not formed as shown below in Figure 16. “Hour Glass” solder joints are a reliability concern and must be avoided.

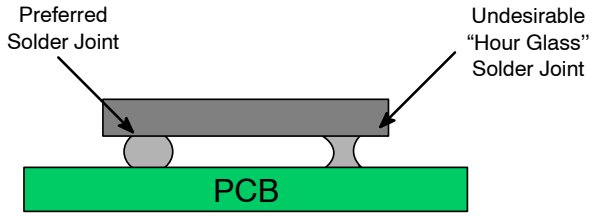


Figure 16. Side View of DFN Illustrating Preferred and Undesirable Solder Joints

Rework Procedure

Due to the fact that the DFN/QFN’s are leadless devices, the entire package must be removed from the PC board if there is an issue with the solder joints. It is important to minimize the chance of overheating neighboring devices during the removal of the package since the devices are typically in close proximity with each other.

Standard SMT rework systems are recommended for this procedure since the airflow and temperature gradients can be carefully controlled. It is also recommend that the PC board be placed in an oven at 125°C for four to eight hours prior to heating the parts to remove excess moisture from the packages. In order to control the region which will be exposed to reflow temperatures, the board should be heated to a 100°C by conduction through the backside of the board in the location of the device. Typically, heating nozzles are then used to increase the temperature locally.

Once the device’s solder joints are heated above their liquidus temperature, the package is quickly removed and the pads on the PC board are cleaned. The cleaning of the pads is typically performed with a blade−style conductive tool with a desoldering braid. A no clean flux is used during this process in order to simplify the procedure.

Solder paste is then deposited or screened onto the site in preparation of mounting a new device. Due to the close proximity of the neighboring packages in most PC board configurations, a miniature stencil for the individual component is typically required. The same stencil design that was originally used to mount the package can be applied to the mini−stencil for redressing the pads.

Due to the small pad configurations of the DFN/QFN, and since the pads are on the underside of the package, a manual pick and place procedure without the aid of magnification is not recommended. A dual image optical system where the underside of the package can be aligned to the PC board should be used instead.

Reflowing the component onto the board can be accomplished by either passing the board through the original reflow profile, or by selectively heating the package with the same process that was used to remove it. The benefit with subjecting the entire board to a second reflow is that the new part will be mounted consistently and by a profile that is already defined. The disadvantage is that all of the other devices mounted with the same solder type will be reflowed for a second time. If subjecting all of the parts to a second reflow is either a concern or unacceptable for a specific application, than the localized reflow option would be the recommended procedure.

AN1040/D

Mounting Considerations for Power Semiconductors

Prepared by: Bill Roehr

ON Semiconductor

http://onsemi.com

APPLICATION NOTE

INTRODUCTION

Current and power ratings of semiconductors are inseparably linked to their thermal environment. Except for lead−mounted parts used at low currents, a heat exchanger is required to prevent the junction temperature from exceeding its rated limit, thereby running the risk of a high failure rate. Furthermore, the semiconductor industry's field history indicated that the failure rate of most silicon semiconductors decreases approximately by one−half for a decrease in junction temperature from 160°C to 135°C.(1) Guidelines for designers of military power supplies impose a 110°C limit upon junction temperature.(2) Proper mounting minimizes the temperature gradient between the semiconductor case and the heat exchanger.

Most early life field failures of power semiconductors can be traced to faulty mounting procedures. With metal packaged devices, faulty mounting generally causes unnecessarily high junction temperature, resulting in reduced component lifetime, although mechanical damage has occurred on occasion from improperly mounting to a warped surface. With the widespread use of various plastic−packaged semiconductors, the prospect of mechanical damage is very significant. Mechanical damage can impair the case moisture resistance or crack the semiconductor die.

Figure 17 shows an example of doing nearly everything wrong. A tab mount TO−220 package is shown being used as a replacement for a TO−213AA (TO−66) part which was socket mounted. To use the socket, the leads are bent − an operation which, if not properly done, can crack the package, break the internal bonding wires, or crack the die. The package is fastened with a sheet−metal screw through a 1/4″ hole containing a fiber−insulating sleeve. The force used to tighten the screw tends to pull the package into the hole, possibly causing enough distortion to crack the die. In addition the contact area is small because of the area consumed by the large hole and the bowing of the package; the result is a much higher junction temperature than expected. If a rough heatsink surface and/or burrs around the hole were displayed in the illustration, most but not all poor mounting practices would be covered.

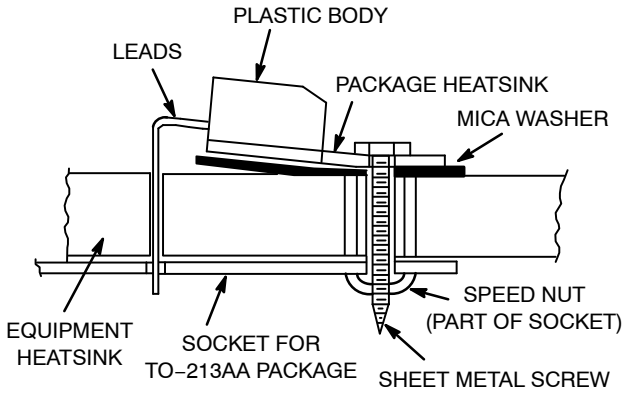


Figure 17. Extreme Case of Improperly Mounting a Semiconductor (Distortion Exaggerated)

In many situations the case of the semiconductor must be electrically isolated from its mounting surface. The isolation material is, to some extent, a thermal isolator as well, which raises junction operating temperatures. In addition, the possibility of arc−over problems is introduced if high voltages are present. Various regulating agencies also impose creepage distance specifications which further complicates design. Electrical isolation thus places additional demands upon the mounting procedure.

Proper mounting procedures usually necessitate orderly attention to the following:

1. Preparing the mounting surface
2. Applying a thermal grease (if required)
3. Installing the insulator (if electrical isolation is desired)
4. Fastening the assembly
5. Connecting the terminals to the circuit

In this note, mounting procedures are discussed in general terms for several generic classes of packages. As newer packages are developed, it is probable that they will fit into the generic classes discussed in this note. Unique requirements are given on data sheets pertaining to the particular package. The following classes are defined:

Stud Mount
Flange Mount
Pressfit
Plastic Body Mount
Tab Mount
Surface Mount

Appendix A contains a brief review of thermal resistance concepts. Appendix B discusses measurement difficulties with interface thermal resistance tests. Appendix C indicates the type of accessories supplied by a number of manufacturers.

MOUNTING SURFACE PREPARATION

In general, the heatsink mounting surface should have a flatness and finish comparable to that of the semiconductor package. In lower power applications, the heatsink surface is satisfactory if it appears flat against a straight edge and is free from deep scratches. In high−power applications, a more detailed examination of the surface is required. Mounting holes and surface treatment must also be considered.

Surface Flatness

Surface flatness is determined by comparing the variance in height (Δh) of the test specimen to that of a reference standard as indicated in Figure 18. Flatness is normally specified as a fraction of the Total Indicator Reading (TIR). The mounting surface flatness, i.e., Δh/TIR, if less than 4 mils per inch, normal for extruded aluminum, is satisfactory in most cases.

Surface Finish

Surface finish is the average of the deviations both above and below the mean value of surface height. For minimum interface resistance, a finish in the range of 50 to 60 microinches is satisfactory; a finer finish is costly to achieve and does not significantly lower contact resistance. Tests conducted by Thermalloy, Inc., using a copper TO−204 (TO−3) package with a typical 32−microinch finish, showed that heatsink finishes between 16 and 64 μ−in caused less than ±2.5% difference in interface thermal resistance when the voids and scratches were filled with a thermal joint compound.[3] Most commercially available cast or extruded heatsinks will require spotfacing when used in high−power applications. In general, milled or machined surfaces are satisfactory if prepared with tools in good working condition.

Mounting Holes

Mounting holes generally should only be large enough to allow clearance of the fastener. The larger thick flange type packages having mounting holes removed from the semiconductor die location, such as the TO−3, may successfully be used with larger holes to accommodate an insulating bushing, but many plastic encapsulated packages are intolerant of this condition. For these packages, a smaller screw size must be used such that the hole for the bushing does not exceed the hole in the package.

Punched mounting holes have been a source of trouble because if not properly done, the area around a punched hole is depressed in the process. This “crater” in the heatsink around the mounting hole can cause two problems. The device can be damaged by distortion of the package as the mounting pressure attempts to conform it to the shape of the heatsink indentation, or the device may only bridge the crater and leave a significant percentage of its heat−dissipating surface out of contact with the heatsink. The first effect may often be detected immediately by visual cracks in the package (if plastic), but usually an unnatural stress is imposed, which results in an early−life failure. The second effect results in hotter operation and is not manifested until much later.

Although punched holes are seldom acceptable in the relatively thick material used for extruded aluminum heatsinks, several manufacturers are capable of properly utilizing the capabilities inherent in both fine−edge blanking or sheared−through holes when applied to sheet metal as commonly used for stamped heatsinks. The holes are pierced using Class A progressive dies mounted on four−post die sets equipped with proper pressure pads and holding fixtures.

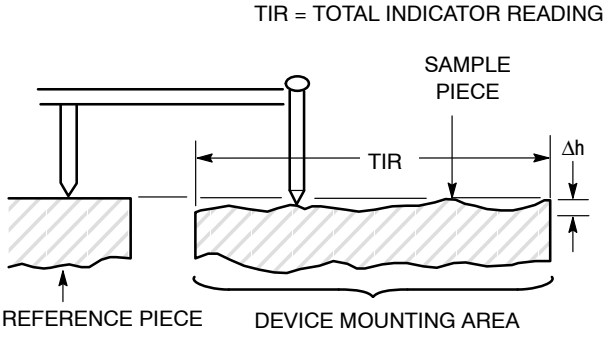


Figure 18. Surface Flatness Measurement

When mounting holes are drilled, a general practice with extruded aluminum, surface cleanup is important. Chamfers must be avoided because they reduce heat transfer surface and increase mounting stress. However, the edges must be broken to remove burrs which cause poor contact between device and heatsink and may puncture isolation material.

Surface Treatment

Many aluminum heatsinks are black−anodized to improve radiation ability and prevent corrosion. Anodizing results in significant electrical but negligible thermal insulation. It need only be removed from the mounting area when electrical contact is required. Heatsinks are also available which have a nickel plated copper insert under the semiconductor mounting area. No treatment of this surface is necessary.

Another treated aluminum finish is iridite, or chromateacid dip, which offers low resistance because of its thin surface, yet has good electrical properties because it resists oxidation. It need only be cleaned of the oils and films that collect in the manufacture and storage of the sinks, a practice which should be applied to all heatsinks.

For economy, paint is sometimes used for sinks; removal of the paint where the semiconductor is attached is usually required because of paint's high thermal resistance. However, when it is necessary to insulate the semiconductor package from the heatsink, hard anodized or painted surfaces allow an easy installation for low voltage applications. Some manufacturers will provide anodized or painted surfaces meeting specific insulation voltage requirements, usually up to 400 volts.

It is also necessary that the surface be free from all foreign material, film, and oxide (freshly bared aluminum forms an oxide layer in a few seconds). Immediately prior to assembly, it is a good practice to polish the mounting area with No. 000 steel wool, followed by an acetone or alcohol rinse.

INTERFACE DECISIONS

When any significant amount of power is being dissipated, something must be done to fill the air voids between mating surfaces in the thermal path. Otherwise the interface thermal resistance will be unnecessarily high and quite dependent upon the surface finishes.

For several years, thermal joint compounds, often called grease, have been used in the interface. They have a resistivity of approximately 60°C/W/in whereas air has 1200°C/W/in. Since surfaces are highly pock−marked with minute voids, use of a compound makes a significant reduction in the interface thermal resistance of the joint. However, the grease causes a number of problems, as discussed in the following section.

To avoid using grease, manufacturers have developed dry conductive and insulating pads to replace the more traditional materials. These pads are conformal and therefore partially fill voids when under pressure.

Thermal Compounds (Grease)

Joint compounds are a formulation of fine zinc or other conductive particles in a silicone oil or other synthetic base fluid which maintains a grease−like consistency with time and temperature. Since some of these compounds do not spread well, they should be evenly applied in a very thin layer using a spatula or lintless brush, and wiped lightly to remove excess material. Some cyclic rotation of the package will help the compound spread evenly over the entire contact area. Some experimentation is necessary to determine the correct quantity; too little will not fill all the voids, while too much may permit some compound to remain between well mated metal surfaces where it will substantially increase the thermal resistance of the joint.

To determine the correct amount, several semiconductor samples and heatsinks should be assembled with different amounts of grease applied evenly to one side of each mating surface. When the amount is correct a very small amount of grease should appear around the perimeter of each mating surface as the assembly is slowly torqued to the recommended value. Examination of a dismantled assembly should reveal even wetting across each mating surface. In production, assemblers should be trained to slowly apply the specified torque even though an excessive amount of grease appears at the edges of mating surfaces. Insufficient torque causes a significant increase in the thermal resistance of the interface.

To prevent accumulation of airborne particulate matter, excess compound should be wiped away using a cloth moistened with acetone or alcohol. These solvents should not contact plastic−encapsulated devices, as they may enter the package and cause a leakage path or carry in substances which might attack the semiconductor chip.

The silicone oil used in most greases has been found to evaporate from hot surfaces with time and become deposited on other cooler surfaces. Consequently, manufacturers must determine whether a microscopically thin coating of silicone oil on the entire assembly will pose any problems. It may be necessary to enclose components using grease. The newer synthetic base greases show far less tendency to migrate or creep than those made with a silicone oil base. However, their currently observed working temperature range are less, they are slightly poorer on thermal conductivity and dielectric strength and their cost is higher.

Data showing the effect of compounds on several package types under different mounting conditions is shown in Figure 1. The rougher the surface, the more valuable the grease becomes in lowering contact resistance; therefore, when mica insulating washers are used, use of grease is generally mandatory. The joint compound also improves the breakdown rating of the insulator.

Conductive Pads

Because of the difficulty of assembly using grease and the evaporation problem, some equipment manufacturers will not, or cannot, use grease. To minimize the need for grease, several vendors offer dry conductive pads which approximate performance obtained with grease. Data for a greased bare joint and a joint using Grafoil®, a dry graphite compound, is shown in the data of Figure 19 through Figure 22. Grafoil is claimed to be a replacement for grease when no electrical isolation is required; the data indicates it does indeed perform as well as grease. Another conductive pad available from Aavid is called Kon−Dux™. It is made with a unique, grain oriented, flake−like structure (patent pending). Highly compressible, it becomes formed to the surface roughness of both the heatsink and semiconductor. Manufacturer's data shows it to provide an interface thermal resistance better than a metal interface with filled silicone grease. Similar dry conductive pads are available from other manufacturers. They are a fairly recent development; long term problems, if they exist, have not yet become evident.

Table 1. Approximate Values for Interface Thermal Resistance Data from Measurements Performed in ON Semiconductor Applications Engineering Laboratory

Dry interface values are subject to wide variation because of extreme dependence upon surface conditions. Unless otherwise noted the case temperature is monitored by a thermocouple located directly under the die reached through a hole in the heatsink. (See Appendix B for a discussion of Interface Thermal Resistance Measurements.)

Package Type and Data		Interface Thermal Resistance (°C/W)						
			Metal−to−Metal		With Insulator			
JEDEC Outlines	Description	Test Torque In−Lb	Dry	Lubed	Dry	Lubed	Type	See Note
DO−203AA, TO−210AA TO−208AB	10−32 Stud 7/16″ Hex	15	0.3	0.2	1.6	0.8	3 mil Mica	
DO−203AB, TO−210AC TO−208	1/4−28 Stud 11/16″ Hex	25	0.2	0.1	0.8	0.6	5 mil Mica	
DO−208AA	Pressfit, 1/2″	−	0.15	0.1	−	−	−	
TO−204AA (TO−3)	Diamond Flange	6	0.5	0.1	1.3	0.36	3 mil Mica	1
TO−213AA (TO−66)	Diamond Flange	6	1.5	0.5	2.3	0.9	2 mil Mica	
TO−126	Thermopad 1/4″ x 3/8″	6	2.0	1.3	4.3	3.3	2 mil Mica	
TO−220AB	Thermowatt	8	1.2	1.0	3.4	1.6	2 mil Mica	1, 2

NOTES: 1. See Figure 19 through Figure 23 for additional data on TO−3 and TO−220 packages.
2. Screw not insulated. See Figure 36.

INSULATION CONSIDERATIONS

Since most power semiconductors use are vertical device construction it is common to manufacture power semiconductors with the output electrode (anode, collector or drain) electrically common to the case; the problem of isolating this terminal from ground is a common one. For lowest overall thermal resistance, which is quite important when high power must be dissipated, it is best to isolate the entire heatsink/semiconductor structure from ground, rather than to use an insulator between the semiconductor and the heatsink. Heatsink isolation is not always possible, however, because of EMI requirements, safety reasons, instances where a chassis serves as a heatsink or where a heatsink is common to several non isolated packages. In these situations insulators are used to isolate the individual components from the heatsink. Newer packages, such as the ON Semiconductor FULLPAK™ and EMS modules, contain the electrical isolation material within, thereby saving the equipment manufacturer the burden of addressing the isolation problem.

Insulator Thermal Resistance

When an insulator is used, thermal grease is of greater importance than with a metal−to−metal contact, because two interfaces exist instead of one and some materials, such as mica, have a hard, markedly uneven surface. With many isolation materials reduction of interface thermal resistance of between 2 to 1 and 3 to 1 are typical when grease is used.

Data obtained by Thermalloy, showing interface resistance for different insulators and torques applied to TO−204 (TO−3) and TO−220 packages, are shown in Figure 19 through Figure 22, for bare and greased surfaces. Similar materials to those shown are available from several manufacturers. It is obvious that with some arrangements, the interface thermal resistance exceeds that of the semiconductor (junction to case).

Referring to Figure 19 through Figure 22, one may conclude that when high power is handled, beryllium oxide is unquestionably the best. However, it is an expensive choice. (It should not be cut or abraded, as the dust is highly toxic.) Thermafilm™ is a filled polymide material which is used for isolation (variation of Kapton®). It is a popular material for low power applications because of its low cost ability to withstand high temperatures, and ease of handling in contrast to mica which chips and flakes easily.

A number of other insulating materials are also shown. They cover a wide range of insulation resistance, thermal resistance and ease of handling. Mica has been widely used in the past because it offers high breakdown voltage and fairly low thermal resistance at a low cost but it certainly should be used with grease.

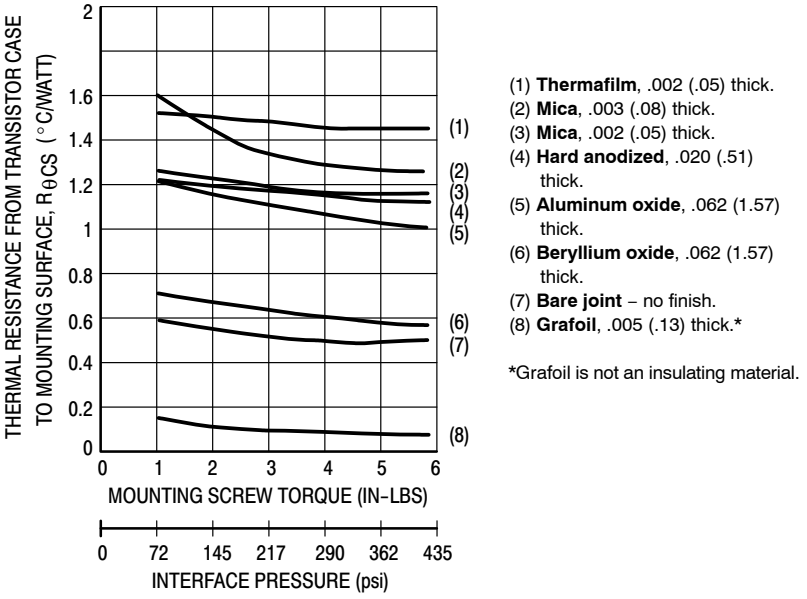


Figure 19. TO−204AA (TO−3) Without Thermal Grease

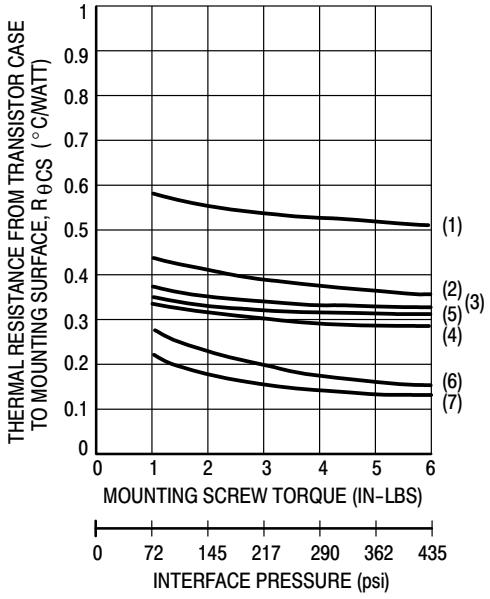


Figure 20. TO−204AA (TO−3) With Thermal Grease

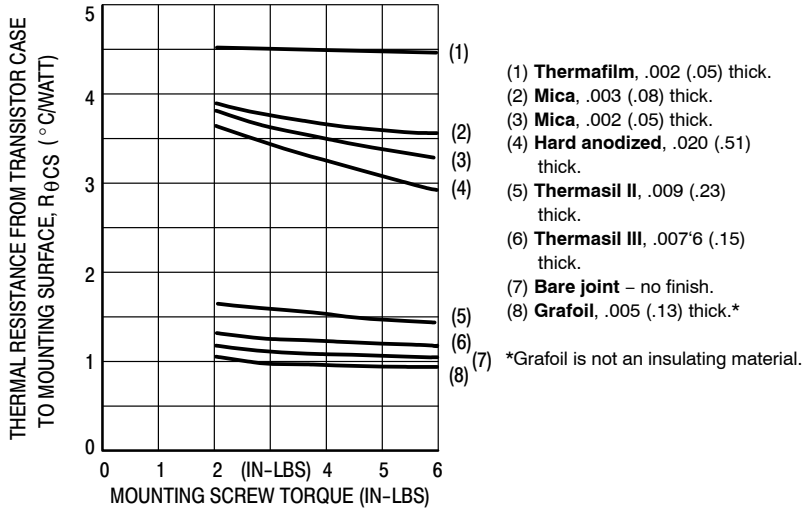


Figure 21. TO−220 Without Thermal Grease

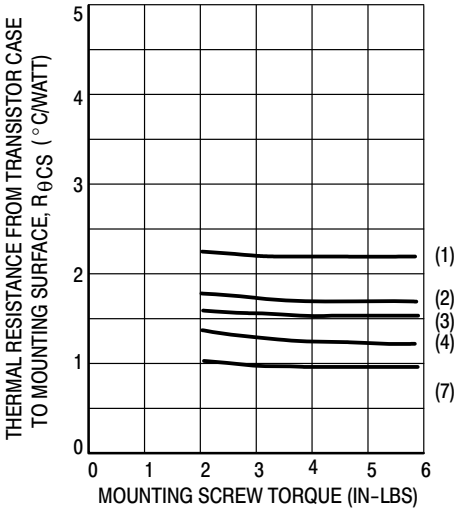


Figure 22. TO−220 With Thermal Grease

INTERFACE THERMAL RESISTANCE FOR TO−204, TO−3 AND TO−220 PACKAGES USING DIFFERENT INSULATING MATERIALS AS A FUNCTION OF MOUNTING SCREW TORQUE (DATA COURTESY THERMALLOY)

Silicone rubber insulators have gained favor because they are somewhat conformal under pressure. Their ability to fill in most of the metal voids at the interface reduces the need for thermal grease. When first introduced, they suffered from cut−through after a few years in service. The ones presently available have solved this problem by having imbedded pads of Kapton or fiberglass. By comparing Figure 21 and Figure 22, it can be noted that Thermasil™, a filled silicone rubber, without grease, has about the same interface thermal resistance as greased mica for the TO−220 package.

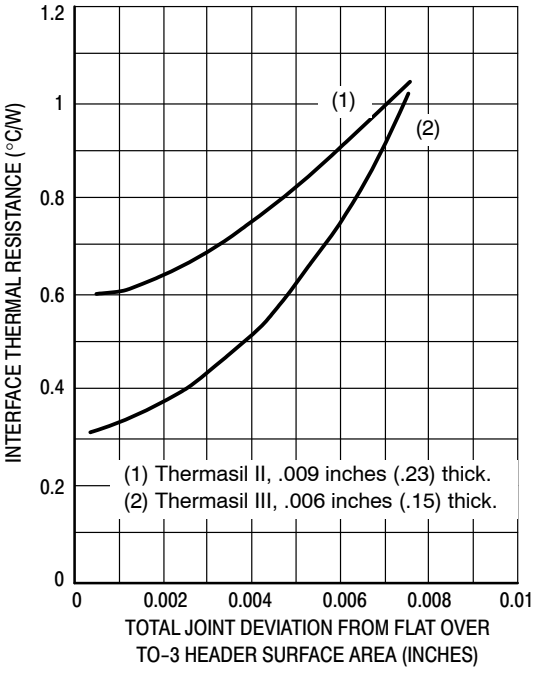
A number of manufacturers offer silicone rubber insulators. Figure 2 shows measured performance of a number of these insulators under carefully controlled, nearly identical conditions. The interface thermal resistance extremes are over 2:1 for the various materials. It is also clear that some of the insulators are much more tolerant than others of out−of−flat surfaces. Since the tests were performed, newer products have been introduced. The Bergquist K−10® pad, for example, is described as having about 2/3 the interface resistance of the Sil Pad® 1000 which would place its performance close to the Chomerics 1671 pad. Aavid also offers an isolated pad called Rubber−Duc™, however it is only available vulcanized to a heatsink and therefore was not included in the comparison. Published data from Aavid shows $R_{\theta CS}$ below 0.3°C/W for pressures above 500 psi. However, surface flatness and other details are not specified so a comparison cannot be made with other data in this note.

Table 2. Thermal Resistance of Silicone Rubber Pads

Manufacturer	Product	$R_{\theta CS}$ @ 3 Mils*	$R_{\theta CS}$ @ 7.5 Mils*
Wakefield	Delta Pad 173−7	.790	1.175
Bergquist	Sil Pad K−4®	.752	1.470
Stockwell Rubber	1867	.742	1.015
Bergquist	Sil Pad 400−9®	.735	1.205
Thermalloy	Thermasil II	.680	1.045
Shin−Etsu	TC−30AG	.664	1.260
Bergquist	Sil Pad 400−7®	.633	1.060
Chomerics	1674	.592	1.190
Wakefield	Delta Pad 174−9	.574	.755
Bergquist	Sil Pad 1000®	.529	.935
Ablestik	Thermal Wafers	.500	.990
Thermalloy	Thermasil III	.440	1.035
Chomerics	1671	.367	.655

*Test Fixture Deviation from flat from Thermalloy EIR86−1010.

The thermal resistance of some silicone rubber insulators is sensitive to surface flatness when used under a fairly rigid base package. Data for a TO−204AA (TO−3) package insulated with Thermasil is shown on Figure 23. Observe that the “worst case” encountered (7.5 mils) yields results having about twice the thermal resistance of the “typical case” (3 mils), for the more conductive insulator. In order for Thermasil III to exceed the performance of greased mica, total surface flatness must be under 2 mils, a situation that requires spot finishing.



Data courtesy of Thermalloy

Figure 23. Effect of Total Surface Flatness on Interface Resistance Using Silicon Rubber Insulators

Silicon rubber insulators have a number of unusual characteristics. Besides being affected by surface flatness and initial contact pressure, time is a factor. For example, in a study of the Cho−Therm® 1688 pad thermal interface impedance dropped from 0.90°C/W to 0.70°C/W at the end of 1000 hours. Most of the change occurred during the first 200 hours where $R_{\theta CS}$ measured 0.74°C/W. The torque on the conventional mounting hardware had decreased to 3 in−lb from an initial 6 in−lb. With nonconformal materials, a reduction in torque would have increased the interface thermal resistance.

Because of the difficulties in controlling all variables affecting tests of interface thermal resistance, data from different manufacturers is not in good agreement. Figure 3 shows data obtained from two sources. The relative performance is the same, except for mica which varies widely in thickness. Appendix B discusses the variables which need to be controlled. At the time of this writing ASTM Committee D9 is developing a standard for interface measurements.

The conclusions to be drawn from all this data is that some types of silicon rubber pads, mounted dry, will out perform the commonly used mica with grease. Cost may be a determining factor in making a selection.

Table 3. Performance of Silicon Rubber Insulators Tested Per MIL−I−49456

Material	Measured Thermal Resistance (°C/W)	
	Thermalloy Data[1]	Bergquist Data[2]
Bare Joint, greased	0.033	0.008
BeO, greased	0.082	–
Cho−Therm, 1617	0.233	–
Q Pad (non−insulated)	–	0.009
Sil Pad, K−10	0.263	0.200
Thermasil III	0.267	–
Mica, greased	0.329	0.400
Sil Pad 1000	0.400	0.300
Cho−Therm 1674	0.433	–
Thermasil II	0.500	–
Sil Pad 400	0.533	0.440
Sil Pad K−4	0.583	0.440

(1) From Thermalloy EIR 87−1030
(2) From Bergquist Data Sheet

Insulation Resistance

When using insulators, care must be taken to keep the mating surfaces clean. Small particles of foreign matter can puncture the insulation, rendering it useless or seriously lowering its dielectric strength. In addition, particularly when voltages higher than 300 V are encountered, problems with creepage may occur. Dust and other foreign material can shorten creepage distances significantly; so having a clean assembly area is important. Surface roughness and humidity also lower insulation resistance. Use of thermal grease usually raises the withstand voltage of the insulation system but excess must be removed to avoid collecting dust. Because of these factors, which are not amenable to analysis, hi−pot testing should be done on prototypes and a large margin of safety employed.

Insulated Electrode Packages

Because of the nuisance of handling and installing the accessories needed for an insulated semiconductor mounting, equipment manufacturers have longed for cost−effective insulated packages since the 1950's. The first to appear were stud mount types which usually have a layer of beryllium oxide between the stud hex and the can. Although effective, the assembly is costly and requires manual mounting and lead wire soldering to terminals on top of the case. In the late eighties, a number of electrically isolated parts became available from various semiconductor manufacturers. These offerings presently consist of multiple chips and integrated circuits as well as the more conventional single chip devices.

The newer insulated packages can be grouped into two categories. The first has insulation between the semiconductor chips and the mounting base; an exposed area of the mounting base is used to secure the part. The EMS (Energy Management Series) Modules, shown on Figure 32, Case 806 (ICePAK™) and Case 388A (TO−258AA) (see Figure 32) are examples of parts in this category. The second category contains parts which have a plastic overmold covering the metal mounting base. The isolated, Case 221C, illustrated in Figure 37, is an example of parts in the second category.

Parts in the first category − those with an exposed metal flange or tab − are mounted the same as their non−insulated counterparts. However, as with any mounting system where pressure is bearing on plastic, the overmolded type should be used with a conical compression washer, described later in this note.

FASTENER AND HARDWARE CHARACTERISTICS

Characteristics of fasteners, associated hardware, and the tools to secure them determine their suitability for use in mounting the various packages. Since many problems have arisen because of improper choices, the basic characteristics of several types of hardware are discussed next.

Compression Hardware

Normal split ring lock washers are not the best choice for mounting power semiconductors. A typical #6 washer flattens at about 50 pounds, whereas 150 to 300 pounds is needed for good heat transfer at the interface. A very useful piece of hardware is the conical, sometimes called a Belleville washer, compression washer. As shown in Figure 24, it has the ability to maintain a fairly constant pressure over a wide range of its physical deflection − generally 20% to 80%. When installing, the assembler applies torque until the washer depresses to half its original height. (Tests should be run prior to setting up the assembly line to determine the proper torque for the fastener used to achieve 50% deflection.) The washer will absorb any cyclic expansion of the package, insulating washer or other materials caused by temperature changes. Conical washers are the key to successful mounting of devices requiring strict control of the mounting force or when plastic hardware is used in the mounting scheme. They are used with the large face contacting the packages. A new variation of the conical washer includes it as part of a nut assembly. Called a "sync nut," the patented device can be soldered to a PC board and the semiconductor mounted with a 6−32 machine screw.[4]

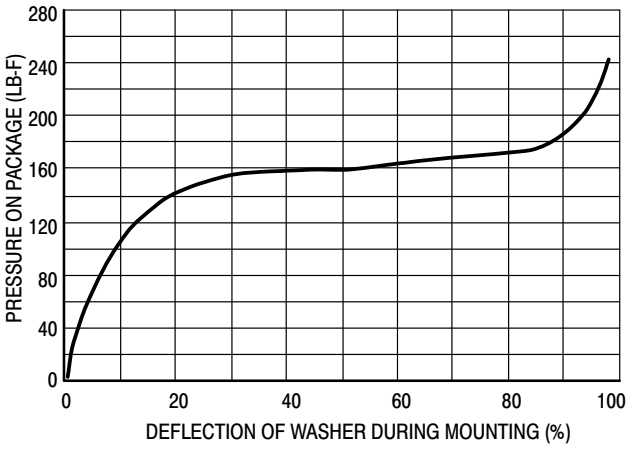


Figure 24. Characteristics of the Conical Compression Washers Designed for Use with Plastic Body Mounted Semiconductors

Clips

Fast assembly is accomplished with clips. When only a few watts are being dissipated, the small board−mounted or free−standing heat dissipaters with an integral clip, offered by several manufacturers, result in a low cost assembly. When higher power is being handled, a separate clip may be used with larger heatsinks. In order to provide proper pressure, the clip must be specially designed for a particular heatsink thickness and semiconductor package.

Clips are especially popular with plastic packages such as the TO−220 and TO−126. In addition to fast assembly, the clip provides lower interface thermal resistance than other assembly methods when it is designed for proper pressure to bear on the top of the plastic over the die. The TO−220 package usually is lifted up under the die location when mounted with a single fastener through the hole in the tab because of the high pressure at one end.

Machine Screws

Machine screws, conical washers, and nuts (or sync nuts) can form a trouble−free fastener system for all types of packages which have mounting holes. However, proper torque is necessary. Torque ratings apply when dry; therefore, care must be exercised when using thermal grease to prevent it from getting on the threads as inconsistent torque readings result. Machine screw heads should not directly contact the surface of plastic packages types as the screw heads are not sufficiently flat to provide properly distributed force. Without a washer, cracking of the plastic case may occur.

Self−Tapping Screws

Under carefully controlled conditions, sheet−metal screws are acceptable. However, during the tapping process with a standard screw, a volcano−like protrusion will develop in the metal being threaded; an unacceptable surface that could increase the thermal resistance may result. When standard sheet metal screws are used, they must be used in a clearance hole to engage a speednut. If a self tapping process is desired, the screw type must be used which roll−forms machine screw threads.

Rivets

Rivets are not a recommended fastener for any of the plastic packages. When a rugged metal flange−mount package or EMS module is being mounted directly to a heatsink, rivets can be used provided press−riveting is used. Crimping force must be applied slowly and evenly. Pop−riveting should never be used because the high crimping force could cause deformation of most semiconductor packages. Aluminum rivets are much preferred over steel because less pressure is required to set the rivet and thermal conductivity is improved.

The hollow rivet, or eyelet, is preferred over solid rivets. An adjustable, regulated pressure press is used such that a gradually increasing pressure is used to pan the eyelet. Use of sharp blows could damage the semiconductor die.

Solder

Until the advent of the surface mount assembly technique, solder was not considered a suitable fastener for power semiconductors. However, user demand has led to the development of new packages for this application. Acceptable soldering methods include conventional belt−furnace, irons, vapor−phase reflow, and infrared reflow. It is important that the semiconductor temperature not exceed the specified maximum (usually 260°C) or the die bond to the case could be damaged. A degraded die bond has excessive thermal resistance which often leads to a failure under power cycling.

Adhesives

Adhesives are available which have coefficients of expansion compatible with copper and aluminum.[5] Highly conductive types are available; a 10 mil layer has approximately 0.3°C/W interface thermal resistance. Different types are offered: high strength types for non−field serviceable systems or low strength types for field serviceable systems. Adhesive bonding is attractive when case mounted parts are used in wave soldering assembly because thermal greases are not compatible with the conformal coatings used and the greases foul the solder process.

Plastic Hardware

Most plastic materials will flow, but differ widely in this characteristic. When plastic materials form parts of the fastening system, compression washers are highly valuable to assure that the assembly will not loosen with time and temperature cycling. As previously discussed, loss of contact pressure will increase interface thermal resistance.

FASTENING TECHNIQUES

Each of the various classes of packages in use requires different fastening techniques. Details pertaining to each type are discussed in following sections. Some general considerations follow.

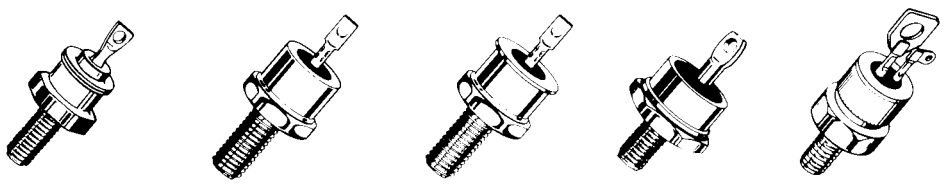
To prevent galvanic action from occurring when devices are used on aluminum heatsinks in a corrosive atmosphere, many devices are nickel− or gold−plated. Consequently, precautions must be taken not to mar the finish.

Another factor to be considered is that when a copper based part is rigidly mounted to an aluminum heatsink, a bimetallic system results which will bend with temperature changes. Not only is the thermal coefficient of expansion different for copper and aluminum, but the temperature gradient through each metal also causes each component to bend. If bending is excessive and the package is mounted by two or more screws the semiconductor chip could be damaged. Bending can be minimized by:

1. Mounting the component parallel to the heatsink fins to provide increased stiffness.
2. Allowing the heatsink holes to be a bit oversized so that some slip between surfaces can occur as temperature changes.
3. Using a highly conductive thermal grease or mounting pad between the heatsink and semiconductor to minimize the temperature gradient and allow for movement.

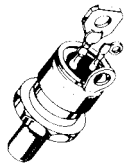
Stud Mount

Parts which fall into the stud−mount classification are shown in Figure 24 through Figure 27. Mounting errors with non−insulated stud−mounted parts are generally confined to application of excessive torque or tapping the stud into a threaded heatsink hole. Both these practices may cause a warpage of the hex base which may crack the semiconductor die. The only recommended fastening method is to use a nut and washer; the details are shown in Figure 28.



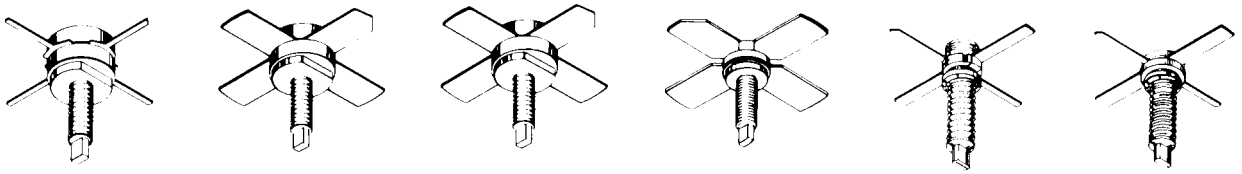
CASE 42A (DO−5) | CASE 56−03 DO−203AA (DO−4) | CASE 245 (DO−4) | CASE 257 DO−203AB (DO−5) | CASE 263−04

Figure 25. Standard Non−Isolated Types



CASE 311−02

Figure 26. Isolated Type



CASE 144B−05 (.380″ STUD) | CASE 145A−09 (.380″ STUD) | CASE 145A−10 (.500″ STUD) | CASE 244−04 (.280″ STUD) | CASE 305−01 (.204″ STUD) | CASE 332−04 (.380″ STUD)

Figure 27. RF Stripline Opposed Emitter (SOE) Series

A VARIETY OF STUD−MOUNT PARTS

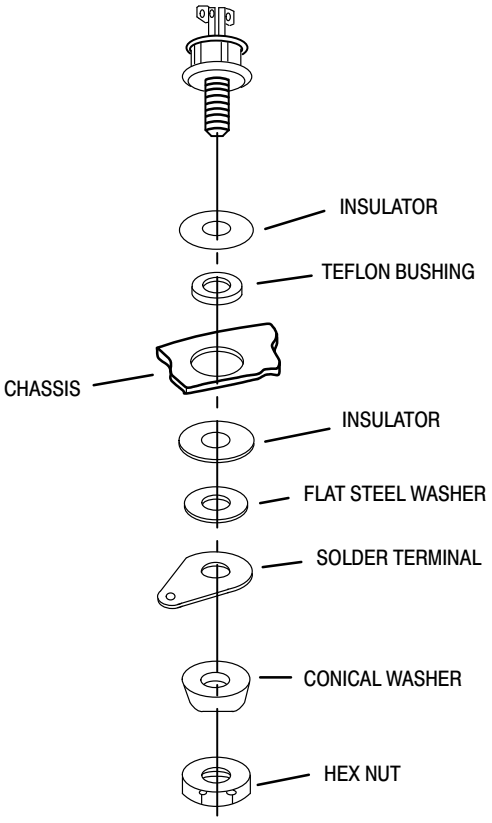


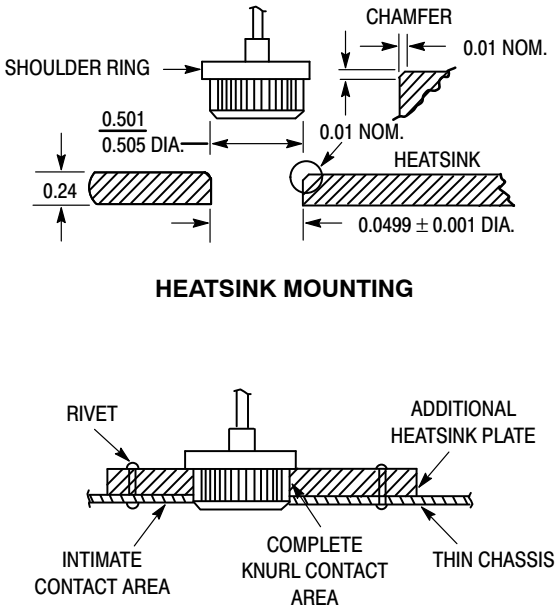
Figure 28. Isolating Hardware Used for a Non−Isolated Stud−Mount Package

Insulated electrode packages on a stud mount base require less hardware. They are mounted the same as their non−insulated counterparts, but care must be exercised to avoid applying a shear or tension stress to the insulation layer, usually a beryllium oxide (BeO) ceramic. This requirement dictates that the leads must be attached to the circuit with flexible wire. In addition, the stud hex should be used to hold the part while the nut is torqued.

RF transistors in the stud−mount stripline opposed emitter (SOE) package impose some additional constraints because of the unique construction of the package. Special techniques to make connections to the stripline leads and to mount the part so no tension or shear forces are applied to any ceramic − metal interface are discussed in the section entitled “Connecting and Handling Terminals.”

Press Fit

For most applications, the press−fit case should be mounted according to the instructions shown in Figure 29. A special fixture meeting the necessary requirements must be used.



HEATSINK MOUNTING

THIN−CHASSIS MOUNTING

The hole edge must be chamfered as shown to prevent shearing off the knurled edge of the case during press−in. The pressing force should be applied evenly on the shoulder ring to avoid tilting or canting of the case in the hole during the pressing operation. Also, the use of a thermal joint compound will be of considerable aid. The pressing force will vary from 250 to 1000 pounds, depending upon the heatsink material. Recommended hardnesses are: copper−less than 50 on the Rockwell F scale; aluminum−less than 65 on the Brinell scale. A heatsink as thin as 1/8″ may be used, but the interface thermal resistance will increase in direct proportion to the contact area. A thin chassis requires the addition of a backup plate.

Figure 29. Press−Fit

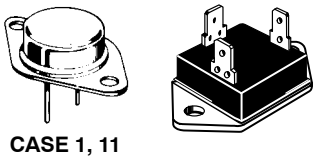
Flange Mount

A large variety of parts fit into the flange mount category as shown in Figure 30 through Figure 33. Few known mounting difficulties exist with the smaller flange mount packages, such as the TO−204 (TO−3). The rugged base and distance between die and mounting holes combine to make it extremely difficult to cause any warpage unless mounted on a surface which is badly bowed or unless one side is tightened excessively before the other screw is started. It is therefore good practice to alternate tightening of the screws so that pressure is evenly applied. After the screws are finger−tight the hardware should be torqued to its final specification in at least two sequential steps. A typical mounting installation for a popular flange type part is shown in Figure 34. Machine screws (preferred) self−tapping screws, eyelets, or rivets may be used to secure the package using guidelines in the previous section, “Fastener and Hardware Characteristics.”

The copper flange of the Energy Management Series (EMS) Modules is very thick. Consequently, the parts are rugged and indestructible for all practical purposes. No special precautions are necessary when fastening these parts to a heatsink.

Some packages specify a tightening procedure. For example, with the Power Tap package, Figure 31, final torque should be applied first to the center position.

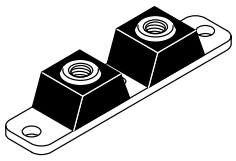
The RF power modules (MHW series) are more sensitive to the flatness of the heatsink than other packages because a ceramic (BeO) substrate is attached to a relatively thin, fairly long, flange. The maximum allowable flange bending to avoid mechanical damage has been determined and presented in detail in Engineering Bulletin EB107/D "Mounting Considerations for ON Semiconductor RF Power Modules." Many of the parts can handle a combined heatsink and flange deviation from flat of 7 to 8 mils which is commonly available. Others must be held to 1.5 mils, which requires that the heatsink have nearly perfect flatness.



CASE 1, 11
TO−204AA
(TO−3)

CASE 383−01

Figure 30. TO−3 Variations



CASE 357C−03

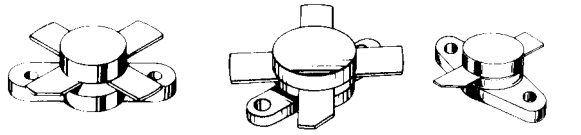
Figure 31. Plastic Power Tap

CASE 373−01 CASE 807−03 CASE 807A−03 CASE 808−01

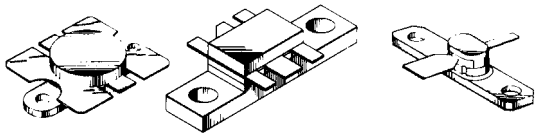
CASE 809−02 CASE 812−02 CASE 813−02

CASE 814−02 CASE 816−02 CASE 819−02

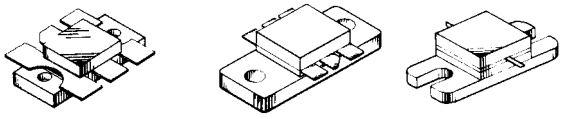
Figure 32. Energy Management Series (Isolated Base Plate)



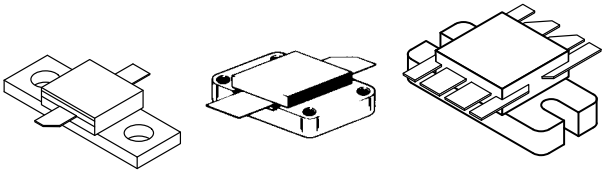
CASE 211−07 CASE 211−11 CASE 215−02



CASE 316−01 CASE 319−07 (CS−12) CASE 328A−03



CASE 333−04 CASE 333A−02 (MAAC PAC) CASE 336−03



CASE 337−02 CASE 368−03 (HOG PAC) CASE 744A−01

Figure 33. RF Stripline Isolated Output Opposed Emitter (SOE) Series

A LARGE ARRAY OF PARTS FIT INTO THE FLANGE−MOUNT CLASSIFICATION

Specific mounting recommendations are critical to RF devices in isolated packages because of the internal ceramic substrate. The large area Case 368−03 (HOG PAC) will be used to illustrate problem areas. It is more sensitive to proper mounting techniques than most other RF power devices.

Although the data sheets contain information on recommended mounting procedures, experience indicates that they are often ignored. For example, the recommended maximum torque on the 4−40 mounting screws is 5 in/lbs. Spring and flat washers are recommended. Over torquing is a common problem. In some parts returned for failure analysis, indentions up to 10 mils deep in the mounting screw areas have been observed.

Calculations indicate that the length of the flange increases in excess of two mils with a temperature change of 75°C. In such cases, if the mounting screw torque is excessive, the flange is prevented from expanding in length, instead it bends upwards in the mid−section, cracking the BeO and the die. A similar result can also occur during the initial mounting of the device if an excessive amount of thermal compound is applied. With

sufficient torque, the thermal compound will squeeze out of the mounting hole areas, but will remain under the center of the flange, deforming it. Deformations of 2 – 3 mils have been measured between the center and the ends under such conditions (enough to crack internal ceramic).

Another problem arises because the thickness of the flange changes with temperature. For the 75°C temperature excursion mentioned, the increased amount is around 0.25 mils which results in further tightening of the mounting screws, thus increasing the effective torque from the initial value. With a decrease in temperature, the opposite effect occurs. Therefore thermal cycling not only causes risk of structural damage but often causes the assembly to loosen which raises the interface resistance. Use of compression hardware can eliminate this problem.

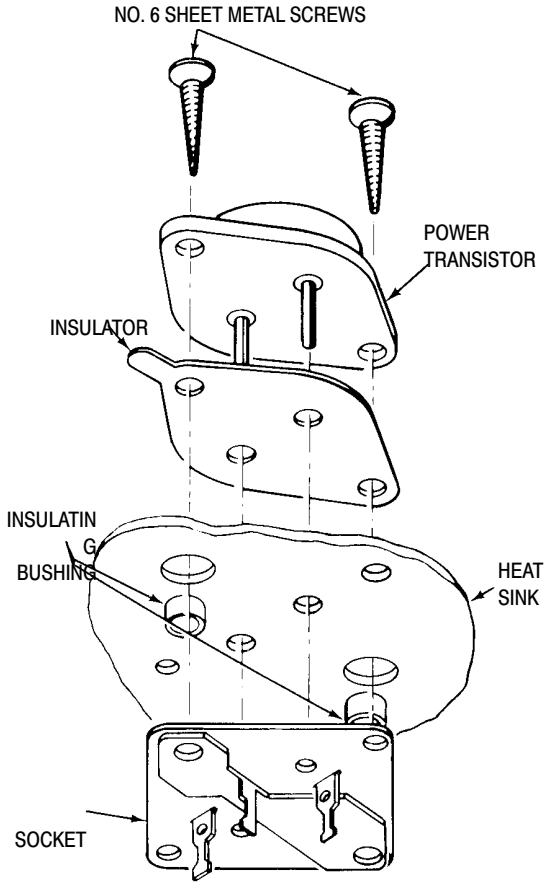


Figure 34. Hardware Used for a TO−204AA (TO−3) Flange Mount Part

Tab Mount

The tab mount class is composed of a wide array of packages as illustrated in Figure 35. Mounting considerations for all varieties are similar to that for the popular TO−220 package, whose suggested mounting arrangements and hardware are shown in Figure 36. The rectangular washer shown in Figure 36a is used to minimize distortion of the mounting flange; excessive distortion could cause damage to the semiconductor chip. Use of the washer is only important when the size of the mounting hole exceeds 0.140 inch (6−32 clearance). Larger holes are needed to accommodate the lower insulating bushing when the screw is electrically connected to the case; however, the holes should not be larger than necessary to provide hardware clearance and should never exceed a diameter of 0.250 inch. Flange distortion is also possible if excessive torque is used during mounting. A maximum torque of 8 inch−pounds is suggested when using a 6−32 screw.

Care should be exercised to assure that the tool used to drive the mounting screw never comes in contact with the plastic body during the driving operation. Such contact can result in damage to the plastic body and internal device connections. To minimize this problem, ON Semiconductor TO−220 packages have a chamfer on one end. TO−220 packages of other manufacturers may need a spacer or combination spacer and isolation bushing to raise the screw head above the top surface of the plastic.

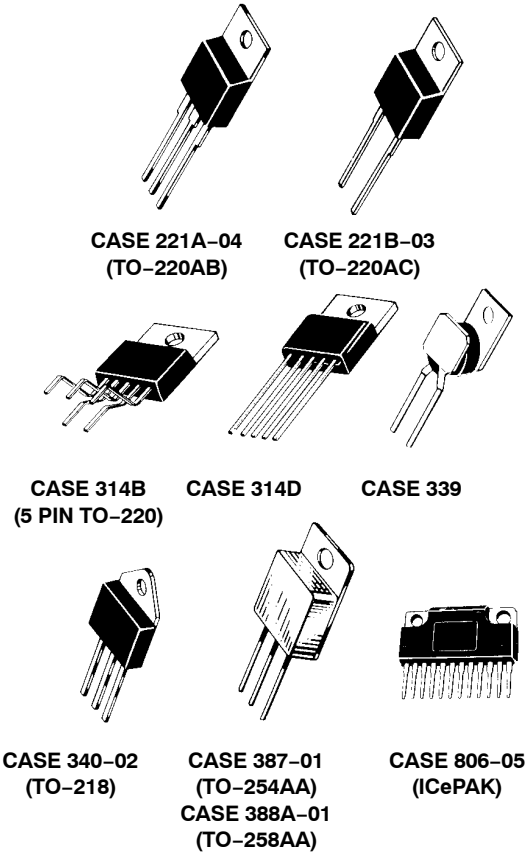


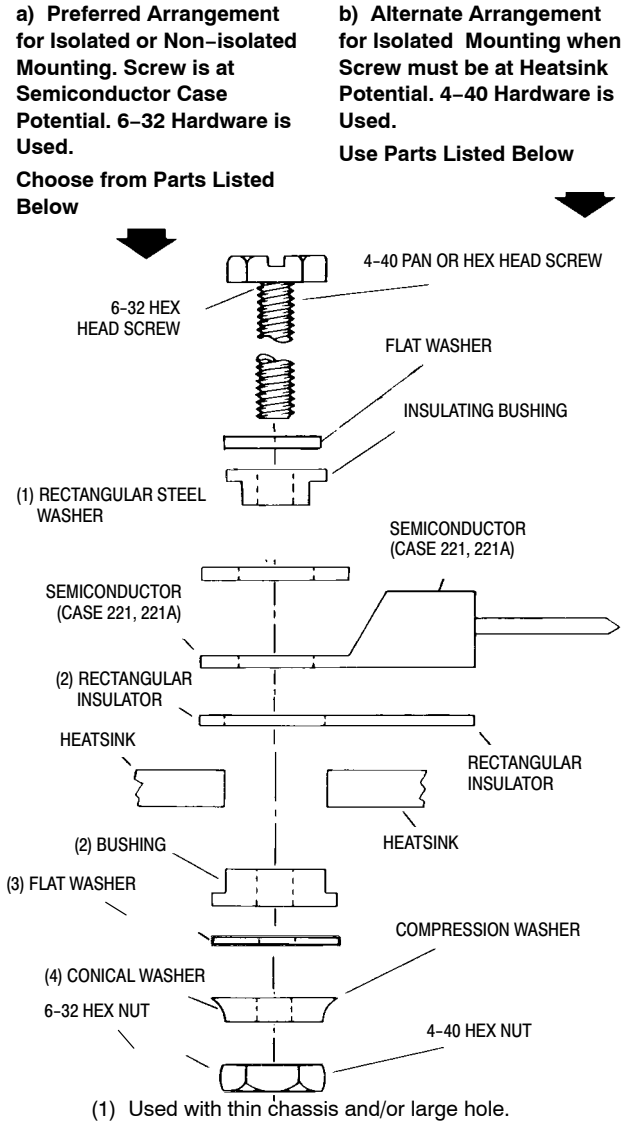
Figure 35. Several Types of Tab−Mount Parts

The popular TO−220 Package and others of similar construction lift off the mounting surface as pressure is applied to one end. (See Appendix B, Figure 52.) To counter this tendency, at least one hardware manufacturer offers a hard plastic cantilever beam which applies more even pressure on the tab.[6] In addition, it separates the mounting screw from the metal tab. Tab mount parts may also be effectively mounted with clips as shown in Figure 43.

To obtain high pressure without cracking the case, a pressure spreader bar should be used under the clip. Interface thermal resistance with the cantilever beam or clips can be lower than with screw mounting.

The ICePAK (Case 806−05) is basically an elongated TO−220 package with isolated chips. The mounting precautions for the TO−220 consequently apply. In addition, since two mounting screws are required, the alternate tightening procedure described for the flange mount package should be used.

In situations where a tab mount package is making direct contact with the heatsink, an eyelet may be used, provided sharp blows or impact shock is avoided.



(1) Used with thin chassis and/or large hole.
(2) Used when isolation is required.
(3) Required when nylon bushing is used.

Figure 36. Mounting Arrangements for Tab Mount TO−220

Plastic Body Mount

The Thermopad™ and isolated plastic power packages shown in Figure 37 are typical of packages in this group. They have been designed to feature minimum size with no compromise in thermal resistance. For the Thermopad (Case 77) parts this is accomplished by die−bonding the silicon chip on one side of a thin copper sheet; the opposite side is exposed as a mounting surface. The copper sheet has a hole for mounting; plastic is molded enveloping the chip but leaving the mounting hole open. The low thermal resistance of this construction is obtained at the expense of a requirement that strict attention be paid to the mounting procedure.

The isolated (Case 221C−02) is similar to a TO−220 except that the tab is encased in plastic. Because the mounting force is applied to plastic, the mounting procedure differs from a standard TO−220 and is similar to that of the Thermopad.

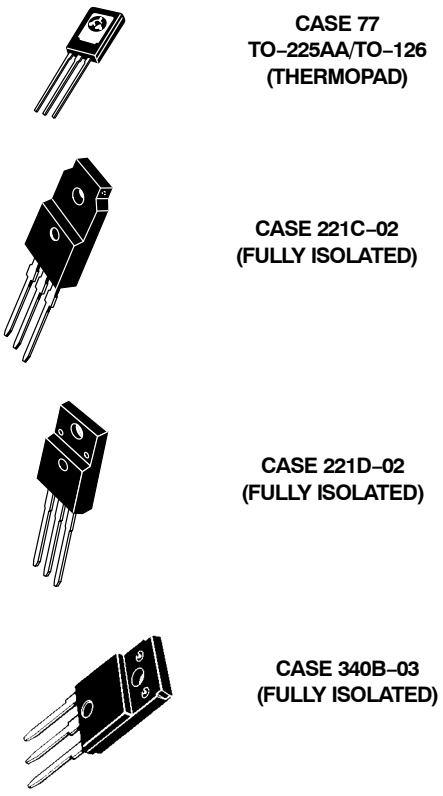


Figure 37. Plastic Body−Mount Packages

Several types of fasteners may be used to secure these packages; machine screws, eyelets, or clips are preferred. With screws or eyelets, a conical washer should be used which applies the proper force to the package over a fairly wide range of deflection and distributes the force over a fairly large surface area. Screws should not be tightened with any type of air−driven torque gun or equipment which may cause high impact. Characteristics of a suitable conical washer is shown in Figure 24.

Figure 38 through Figure 40 shows details of mounting Case 77 devices. Clip mounting is fast and requires minimum hardware, however, the clip must be properly chosen to insure that the proper mounting force is applied. When electrical isolation is required with screw mounting, a bushing inside the mounting hole will insure that the screw threads do not contact the metal base.

The isolated, (Case 221C, 221D and 340B) permits the mounting procedure to be greatly simplified over that of a standard TO−220. As shown in Figure 43, one properly chosen clip, inserted into two slotted holes in the heatsink, is all the hardware needed. Even though clip pressure is much lower than obtained with a screw, the thermal resistance is about the same for either method. This occurs because the clip bears directly on top of the die and holds the package flat while the screw causes the package to lift up somewhat under the die. (See Figure 52 of Appendix B.) The interface should consist of a layer of thermal grease or a highly conductive thermal pad. Of course, screw mounting shown in Figure 42 may also be used but a conical compression washer should be included. Both methods afford a major reduction in hardware as compared to the conventional mounting method with a TO−220 package which is shown in Figure 41.

Surface Mount

Although many of the tab mount parts have been surface mounted, special small footprint packages for mounting power semiconductors using surface mount assembly techniques have been developed. The DPAK, shown in Figure 44, for example, will accommodate a die up to 112 mils x 112 mils, and has a typical thermal resistance around 2°C/W junction to case. The thermal resistance values of the solder interface is well under 1°C/W. The printed circuit board also serves as the heatsink.

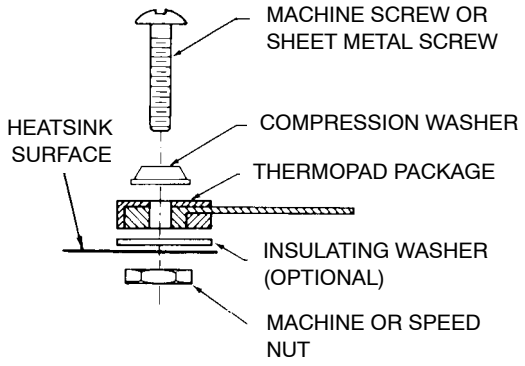
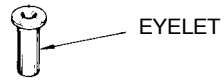


Figure 38. Machine Screw Mounting



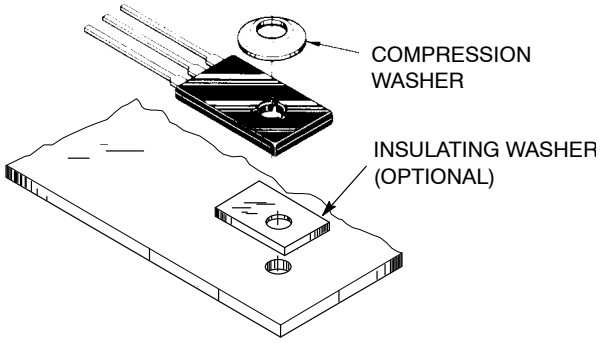


Figure 39. Eyelet Mounting

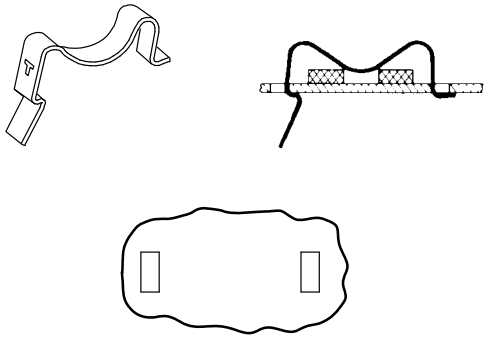


Figure 40. Clips

RECOMMENDED MOUNTING ARRANGEMENTS FOR TO−225AA (TO−126) THERMOPAD PACKAGES

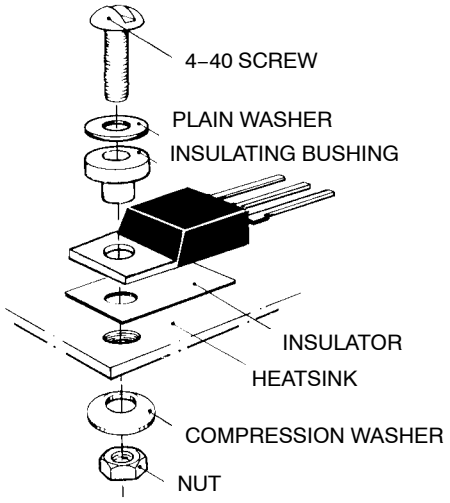


Figure 41. Screw−Mounted TO−220

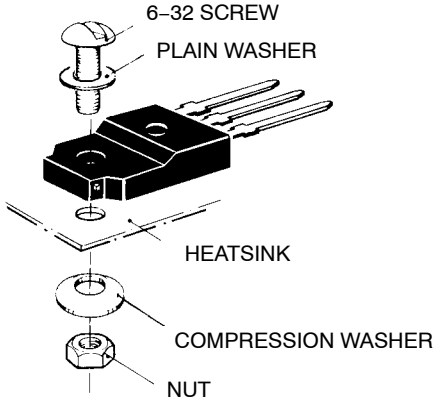


Figure 42. Screw−Mounted Isolated Package

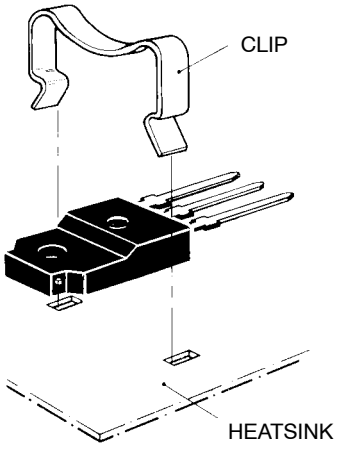


Figure 43. Clip−Mounted Isolated Package

MOUNTING ARRANGEMENTS FOR THE ISOLATED PACKAGE AS COMPARED TO A CONVENTIONAL

CASE 369−07 CASE 369A−13

Figure 44. Surface Mount D−PAK Parts

Standard Glass−Epoxy 2−ounce boards do not make very good heatsinks because the thin foil has a high thermal resistance. As Figure 45 shows, thermal resistance asymptotes to about 20°C/W at 10 square inches of board area, although a point of diminishing returns occurs at about 3 square inches.

Boards are offered that have thick aluminum or copper substrates. A dielectric coating designed for low thermal resistance is overlaid with one or two ounce copper foil for the preparation of printed conductor traces. Tests run on such a product indicate that case to substrate thermal resistance is in the vicinity of 1°C/W, exact values depending upon board type.(7) The substrate may be an effective heatsink itself, or it can be attached to a conventional finned heatsink for improved performance.

Since DPAK and other surface mount packages are designed to be compatible with surface mount assembly techniques, no special precautions are needed other than to insure that maximum temperature/time profiles are not exceeded.

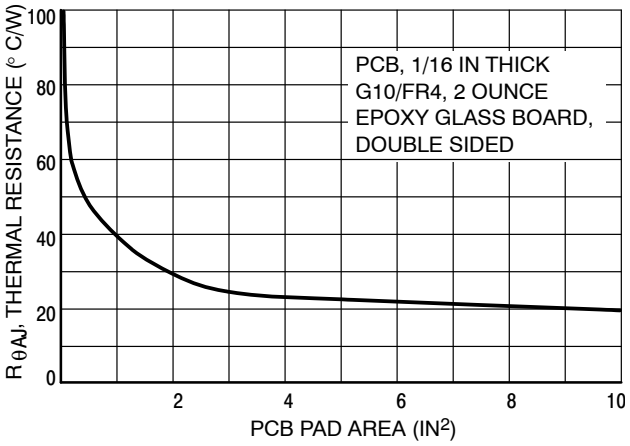


Figure 45. Effect of Footprint Area on Thermal Resistance of DPAK Mounted on a Glass−Epoxy Board

FREE AIR AND SOCKET MOUNTING

In applications where average power dissipation is on the order of a watt or so, most power semiconductors may be mounted with little or no heatsinking. The leads of the various metal power packages are not designed to support the packages; their cases must be firmly supported to avoid the possibility of cracked seals around the leads. Many plastic packages may be supported by their leads in applications where high shock and vibration stresses are not encountered and where no heatsink is used. The leads should be as short as possible to increase vibration resistance and reduce thermal resistance. As a general practice however, it is better to support the package. A plastic support for the TO−220 Package and other similar types is offered by heatsink accessory vendors.

In many situations, because its leads are fairly heavy, the Case 77 (TO−225AA) (TO−127) package has supported a small heatsink; however, no definitive data is available. When using a small heatsink, it is good practice to have the sink rigidly mounted such that the sink or the board is providing total support for the semiconductor. Two possible arrangements are shown in Figure 46 and Figure 47. The arrangement of Figure 46 could be used with any plastic package, but the scheme of Figure 47 is more practical with Case 77 Thermopad devices. With the other package types, mounting the transistor on top of the heatsink is more practical.

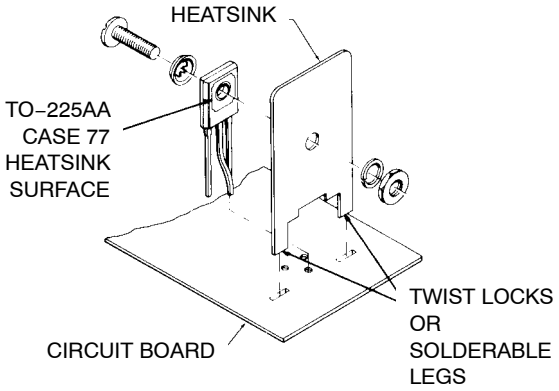


Figure 46. Simple Plate, Vertically Mounted

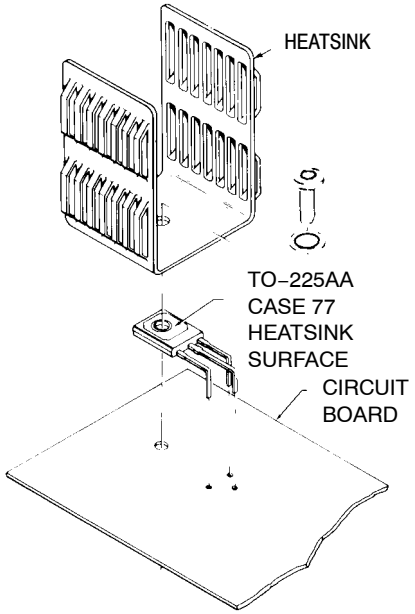


Figure 47. Commercial Sink, Horizontally Mounted

METHODS OF USING SMALL HEATSINKS WITH PLASTIC SEMICONDUCTOR PACKAGES

In certain situations, in particular where semiconductor testing is required or prototypes are being developed, sockets are desirable. Manufacturers have provided sockets for many of the packages available from ON Semiconductor. The user is urged to consult manufacturers' catalogs for specific details. Sockets with Kelvin connections are necessary to obtain accurate voltage readings across semiconductor terminals.

CONNECTING AND HANDLING TERMINALS

Pins, leads, and tabs must be handled and connected properly to avoid undue mechanical stress which could cause semiconductor failure. Change in mechanical dimensions as a result of thermal cycling over operating temperature extremes must be considered. Standard metal, plastic, and RF stripline packages each have some special considerations.

Metal Packages

The pins and lugs of metal packaged devices using glass to metal seals are not designed to handle any significant bending or stress. If abused, the seals could crack. Wires may be attached using sockets, crimp connectors or solder, provided the data sheet ratings are observed. When wires are attached directly to the pins, flexible or braided leads are recommended in order to provide strain relief.

EMS Modules

The screw terminals of the EMS modules look deceptively rugged. Since the flange base is mounted to a rigid heatsink, the connection to the terminals must allow some flexibility. A rigid buss bar should not be bolted to terminals. Lugs with braid are preferred.

Plastic Packages

The leads of the plastic packages are somewhat flexible and can be reshaped although this is not a recommended procedure. In many cases, a heatsink can be chosen which makes lead−bending unnecessary. Numerous lead and tab−forming options are available from ON Semiconductor on large quantity orders. Preformed leads remove the users risk of device damage caused by bending.

If, however, lead−bending is done by the user, several basic considerations should be observed. When bending the lead, support must be placed between the point of bending and the package. For forming small quantities of units, a pair of pliers may be used to clamp the leads at the case, while bending with the fingers or another pair of pliers. For production quantities, a suitable fixture should be made.

The following rules should be observed to avoid damage to the package.

1. A leadbend radius greater than 1/16 inch is advisable for TO−225AA (Case 77) and 1/32 inch for TO−220.
2. No twisting of leads should be done at the case.
3. No axial motion of the lead should be allowed with respect to the case.

The leads of plastic packages are not designed to withstand excessive axial pull. Force in this direction greater than 4 pounds may result in permanent damage to the device. If the mounting arrangement imposes axial stress on the leads, a condition which may be caused by thermal cycling, some method of strain relief should be devised. When wires are used for connections, care should be exercised to assure that movement of the wire does not cause movement of the lead at the lead−to−plastic junctions. Highly flexible or braided wires are good for providing strain relief.

Wire−wrapping of the leads is permissible, provided that the lead is restrained between the plastic case and the point of the wrapping. The leads may be soldered; the maximum soldering temperature, however, must not exceed 260°C and must be applied for not more than 5 seconds at a distance greater than 1/8 inch from the plastic case.

Stripline Packages

The leads of stripline packages normally are soldered into a board while the case is recessed to contact a heatsink as shown in Figure 48 through Figure 50. The following rules should be observed:

1. The device should never be mounted in such a manner as to place ceramic−to−metal joints in tension.
2. The device should never be mounted in such a manner as to apply force on the strip leads in a vertical direction towards the cap.
3. When the device is mounted in a printed circuit board with the copper stud and BeO portion of the header passing through a hole in the circuit boards, adequate clearance must be provided for the BeO to prevent shear forces from being applied to the leads.
4. Some clearance must be allowed between the leads and the circuit board when the device is secured to the heatsink.
5. The device should be properly secured into the heatsinks before its leads are attached into the circuit.
6. The leads on stud type devices must not be used to prevent device rotation during stud torque application. A wrench flat is provided for this purpose.

Figure 49 shows a cross−section of a printed circuit board and heatsink assembly for mounting a stud type stripline device. H is the distance from the top surface of the printed circuit board to the D−flat heatsink surface. If H is less than the minimum distance from the bottom of the lead material to the mounting surface of the package, there is no possibility of tensile forces in the copper stud − BeO ceramic joint. If, however, H is greater than the package dimension, considerable force is applied to the cap to BeO joint and the BeO to stud joint. Two occurrences are possible at this point. The first is a cap joint failure when the structure is heated, as might occur during the lead−soldering operation; while the second is BeO to stud failure if the force generated is high enough. Lack of contact between the device and the heatsink surface will occur as the differences between H and the package dimension become larger, this may result in device failure as power is applied.

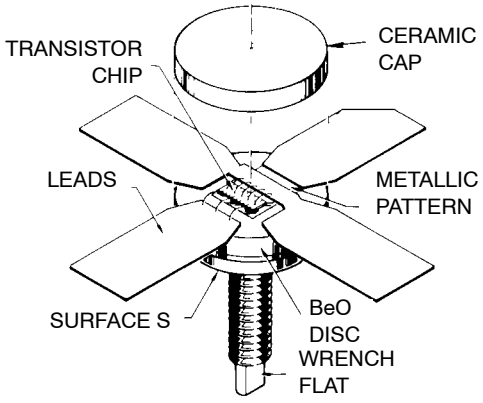


Figure 48. Component Parts of a Stud Mount Stripline Package. Flange Mounted Packages are Similarly Constructed

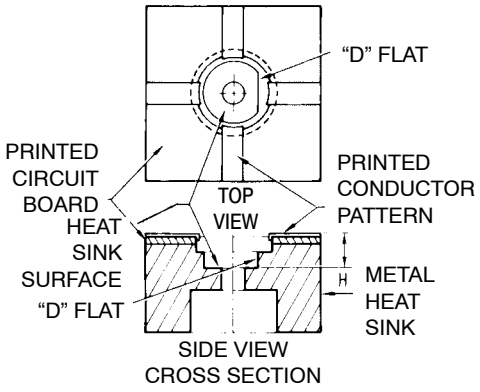


Figure 49. Typical Stud Type SOE Transistor Mounting Method

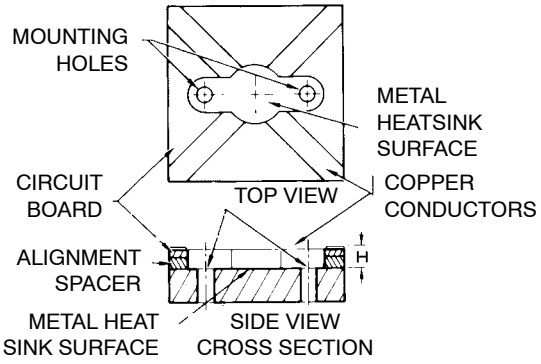


Figure 50. Flange Type SOE Transistor Mounting Method

MOUNTING DETAILS FOR SOE TRANSISTORS

Figure 50 shows a typical mounting technique for flange−type stripline transistors. Again, H is defined as the distance from the top of the printed circuit board to the heatsink surface. If distance H is less than the minimum distance from the bottom of transistor lead to the bottom surface of the flange, tensile forces at the various joints in the package are avoided. However, if distance H exceeds the package dimension, problems similar to those discussed for the stud type devices can occur.

CLEANING CIRCUIT BOARDS

It is important that any solvents or cleaning chemicals used in the process of degreasing or flux removal do not affect the reliability of the devices. Alcohol and unchlorinated Freon solvents are generally satisfactory for use with plastic devices, since they do not damage the package. Hydrocarbons such as gasoline and chlorinated Freon may cause the encapsulant to swell, possibly damaging the transistor die.

When using an ultrasonic cleaner for cleaning circuit boards, care should be taken with regard to ultrasonic energy and time of application. This is particularly true if any packages are free−standing without support.

THERMAL SYSTEM EVALUATION

Assuming that a suitable method of mounting the semiconductor without incurring damage has been achieved, it is important to ascertain whether the junction temperature is within bounds.

In applications where the power dissipated in the semiconductor consists of pulses at a low duty cycle, the instantaneous or peak junction temperature, not average temperature, may be the limiting condition. In this case, use must be made of transient thermal resistance data. For a full explanation of its use, see ON Semiconductor Application Note, AN569/D.

Other applications, notably RF power amplifiers or switches driving highly reactive loads, may create severe current crowding conditions which render the traditional concepts of thermal resistance or transient thermal impedance invalid. In this case, transistor safe operating area, thyristor di/dt limits, or equivalent ratings as applicable, must be observed.

Fortunately, in many applications, a calculation of the average junction temperature is sufficient. It is based on the concept of thermal resistance between the junction and a temperature reference point on the case. (See Appendix A.) A fine wire thermocouple should be used, such as #36 AWG, to determine case temperature. Average operating junction temperature can be computed from the following equation:

$$T_J = T_C + R_{\theta JC} \times P_D$$

where T_J = junction temperature (°C)
T_C = case temperature (°C)
$R_{\theta JC}$ = thermal resistance junction−to case as specified on the data sheet (°C/W)
P_D = power dissipated in the device (W)

The difficulty in applying the equation often lies in determining the power dissipation. Two commonly used empirical methods are graphical integration and substitution.

Graphical Integration

Graphical integration may be performed by taking oscilloscope pictures of a complete cycle of the voltage and current waveforms, using a limit device. The pictures should be taken with the temperature stabilized. Corresponding points are then read from each photo at a suitable number of time increments. Each pair of voltage and current values are multiplied together to give instantaneous values of power. The results are plotted on linear graph paper, the number of squares within the curve counted, and the total divided by the number of squares along the time axis. The quotient is the average power dissipation. Oscilloscopes are available to perform these measurements and make the necessary calculations.

Substitution

This method is based upon substituting an easily measurable, smooth dc source for a complex waveform. A switching arrangement is provided which allows operating the load with the device under test, until it stabilizes in temperature. Case temperature is monitored. By throwing the switch to the “test” position, the device under test is connected to a dc power supply, while another pole of the switch supplies the normal power to the load to keep it operating at full power level. The dc supply is adjusted so that the semiconductor case temperature remains approximately constant when the switch is thrown to each position for about 10 seconds. The dc voltage and current values are multiplied together to obtain average power. It is generally necessary that a Kelvin connection be used for the device voltage measurement.

APPENDIX A
THERMAL RESISTANCE CONCEPTS

The basic equation for heat transfer under steady−state conditions is generally written as:

$$q = hA\Delta T \quad (1)$$

where q = rate of heat transfer or power dissipation (P_D)
h = heat transfer coefficient,
A = area involved in heat transfer,
ΔT = temperature difference between regions of heat transfer.

However, electrical engineers generally find it easier to work in terms of thermal resistance, defined as the ratio of temperature to power. From Equation 1, thermal resistance, R_θ, is

$$R_\theta = \Delta T/q = 1/hA \quad (2)$$

The coefficient (h) depends upon the heat transfer mechanism used and various factors involved in that particular mechanism.

An analogy between Equation (2) and Ohm's Law is often made to form models of heat flow. Note that T could be thought of as a voltage thermal resistance corresponds to electrical resistance (R); and, power (q) is analogous to current (I). This gives rise to a basic thermal resistance model for a semiconductor as indicated by Figure 51.

The equivalent electrical circuit may be analyzed by using Kirchoff's Law and the following equation results:

$$T_J = P_D (R_{\theta JC} + P_{\theta CS} + R_{\theta SA}) + T_A \quad (3)$$

where T_J = junction temperature,
PD = power dissipation
$R_{\theta JC}$ = semiconductor thermal resistance (junction to case),
$R_{\theta CS}$ = interface thermal resistance (case to heat−sink),
$R_{\theta SA}$ = heat sink thermal resistance (heatsink to ambient),
T_A = ambient temperature.

The thermal resistance junction to ambient is the sum of the individual components. Each component must be minimized if the lowest junction temperature is to result.

The value for the interface thermal resistance, $R_{\theta CS}$, may be significant compared to the other thermal resistance terms. A proper mounting procedure can minimize $R_{\theta CS}$.

The thermal resistance of the heatsink is not absolutely constant; its thermal efficiency increases as ambient temperature increases and it is also affected by orientation of the sink. The thermal resistance of the semiconductor is also variable; it is a function of biasing and temperature. Semiconductor thermal resistance specifications are normally at conditions where current density is fairly uniform. In some applications such as in RF power amplifiers and short−pulse applications, current density is not uniform and localized heating in the semiconductor chip will be the controlling factor in determining power handling ability.

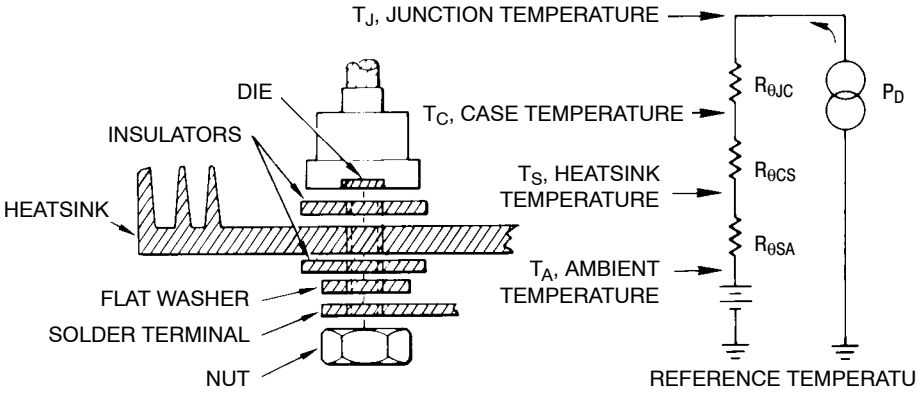


Figure 51. Basic Thermal Resistance Model Showing Thermal to Electrical Analogy for a Semiconductor

APPENDIX B
MEASUREMENT OF INTERFACE THERMAL RESISTANCE

Measuring the interface thermal resistance $R_{\theta CS}$ appears deceptively simple. All that's apparently needed is a thermocouple on the semiconductor case, a thermocouple on the heatsink, and a means of applying and measuring DC power. However, $R_{\theta CS}$ is proportional to the amount of contact area between the surfaces and consequently is affected by surface flatness and finish and the amount of pressure on the surfaces. The fastening method may also be a factor. In addition, placement of the thermocouples can have a significant influence upon the results. Consequently, values for interface thermal resistance presented by different manufacturers are not in good agreement. Fastening methods and thermocouple locations are considered in this Appendix.

When fastening the test package in place with screws, thermal conduction may take place through the screws, for example, from the flange ear on a TO−3 package directly to the heatsink. This shunt path yields values which are artificially low for the insulation material and dependent upon screw head contact area and screw material. MIL−I−49456 allows screws to be used in tests for interface thermal resistance probably because it can be argued that this is "application oriented."

Thermalloy takes pains to insulate all possible shunt conduction paths in order to more accurately evaluate insulation materials. The ON Semiconductor fixture uses an insulated clamp arrangement to secure the package which also does not provide a conduction path.

As described previously, some packages, such as a TO−220, may be mounted with either a screw through the tab or a clip bearing on the plastic body. These two methods often yield different values for interface thermal resistance. Another discrepancy can occur if the top of the package is exposed to the ambient air where radiation and convection can take place. To avoid this, the package should be covered with insulating foam. It has been estimated that a 15 to 20% error in $R_{\theta CS}$ can be incurred from this source.

Another significant cause for measurement discrepancies is the placement of the thermocouple to measure the semiconductor case temperature. Consider the TO−220 package shown in Figure 52. The mounting pressure at one end causes the other end − where the die is located − to lift off the mounting surface slightly. To improve contact, ON Semiconductor TO−220 Packages are slightly concave. Use of a spreader bar under the screw lessens the lifting, but some is inevitable with a package of this structure. Three thermocouple locations are shown:

1. The ON Semiconductor location is directly under the die reached through a hole in the heatsink. The thermocouple is held in place by a spring which forces the thermocouple into intimate contact with the bottom of the semi's case.
2. The JEDEC location is close to the die on the top surface of the package base reached through a blind hole drilled through the molded body. The thermocouple is swaged in place.
3. The Thermalloy location is on the top portion of the tab between the molded body and the mounting screw. The thermocouple is soldered into position.

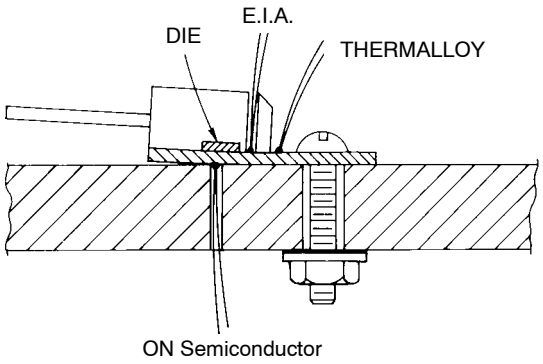


Figure 52. JEDEC TO−220 Package Mounted to Heatsink Showing Various Thermocouple Locations and Lifting Caused by Pressure at One End

Temperatures at the three locations are generally not the same. Consider the situation depicted in the figure. Because the only area of direct contact is around the mounting screw, nearly all the heat travels horizontally along the tab from the die to the contact area. Consequently, the temperature at the JEDEC location is hotter than at the Thermalloy location and the ON Semiconductor location is even hotter. Since junction−to−sink thermal resistance must be constant for a given test setup, the calculated junction−to−case thermal resistance values decrease and case−to−sink values increase as the "case" temperature thermocouple readings become warmer. Thus the choice of reference point for the "case" temperature is quite important.

There are examples where the relationship between the thermocouple temperatures are different from the previous situation. If a mica washer with grease is installed between the semiconductor package and the heatsink, tightening the screw will not bow the package; instead, the mica will be deformed. The primary heat conduction path is from the die through the mica to the heatsink. In this case, a small temperature drop will exist across the vertical dimension of the package mounting base so that the thermocouple at the EIA location will be the hottest. The thermocouple temperature at the Thermalloy location will be lower but close to the temperature at the EIA location as the lateral heat flow is generally small. The ON Semiconductor location will be coolest.

The EIA location is chosen to obtain the highest temperature on the case. It is of significance because power ratings are supposed to be based on this reference point. Unfortunately, the placement of the thermocouple is tedious and leaves the semiconductor in a condition unfit for sale.

The ON Semiconductor location is chosen to obtain the highest temperature of the case at a point where, hopefully, the case is making contact to the heatsink. Once the special heatsink to accommodate the thermocouple has been fabricated, this method lends itself to production testing and does not mark the device. However, this location is not easily accessible to the user.

The Thermalloy location is convenient and is often chosen by equipment manufacturers. However, it also blemishes the case and may yield results differing up to 1°C/W for a TO−220 package mounted to a heatsink without thermal grease and no insulator. This error is small when compared to the thermal resistance of heat dissipaters often used with this package, since power dissipation is usually a few watts. When compared to the specified junction−to−case values of some of the higher power semiconductors becoming available, however, the difference becomes significant and it is important that the semiconductor manufacturer and equipment manufacturer use the same reference point.

Another EIA method of establishing reference temperatures utilizes a soft copper washer (thermal grease is used) between the semiconductor package and the heatsink. The washer is flat to within 1 mil/inch, has a finish better than 63 μ−inch, and has an imbedded thermocouple near its center. This reference includes the interface resistance under nearly ideal conditions and is therefore application−oriented. It is also easy to use but has not become widely accepted.

A good way to improve confidence in the choice of case reference point is to also test for junction−to−case thermal resistance while testing for interface thermal resistance. If the junction−to−case values remain relatively constant as insulators are changed, torque varied, etc., then the case reference point is satisfactory.

APPENDIX C
Sources of Accessories

Manufacturer	Joint Compound	Adhesives	Insulators						Heatsinks	Clips
			BeO	AlO_2	Anodize	Mica	Plastic Film	Silicone Rubber		
Aavid	–	–	–	–	–	–	X	X	X	X
AHAM−TOR	–	–	–	–	–	–	–	–	X	–
Asheville−Schoonmaker	–	–	–	–	–	X	–	–	–	–
Astrodynamis	X	–	–	–	–	–	–	–	X	–
Delbert Blinn	–	–	X	–	X	X	X	X	X	–
IERC	X	–	–	–	–	–	–	–	X	–
Staver	–	–	–	–	–	–	–	–	X	–
Thermalloy	X	X	X	X	X	X	X	X	X	X
Tran−tec	X	–	X	X	X	X	–	X	X	–
Wakefield	X	X	X	–	X	–	–	X	X	X

Other Sources for silicone rubber pads: Chomerics, Bergquist

Suppliers Addresses

Aavid Engineering, Inc., P.O. Box 400, Laconia, New Hampshire 03247 (603) 524−1478
AHAM−TOR Heatsinks, 27901 Front Street, Rancho, California 92390 (714) 676−4151
Asheville−Schoonmaker, 900 Jefferson Ave., Newport News, VA 23607 (804) 244−7311
Astro Dynamics, Inc., 2 Gill St., Woburn, Massachusetts 01801 (617) 935−4944
Bergquist, 5300 Edina Industrial Blvd., Minneapolis, Minnesota 55435 (612) 835−2322
Chomerics, Inc.,16 Flagstone Drive, Hudson, New Hampshire 03051 1−800−633−8800
Delbert Blinn Company, P.O. Box 2007, Pomona, California 91769 (714) 623−1257
International Electronic Research Corporation, 135 West Magnolia Boulevard, Burbank, California 91502 (213) 849−2481
The Staver Company, Inc., 41−51 Saxon Avenue, Bay Shore, Long Island, New York 11706 (516) 666−8000
Thermalloy, Inc., P.O. Box 34829, 2021 West Valley View Lane, Dallas, Texas 75234 (214) 243−4321
Tran−tec Corporation, P.O. Box 1044, Columbus, Nebraska 68601 (402) 564−2748
Wakefield Engineering, Inc., Wakefield, Massachusetts 01880 (617) 245−5900

PACKAGE INDEX

PREFACE

When the JEDEC registration system for package outlines started in 1957, numbers were assigned sequentially whenever manufacturers wished to establish a package as an industry standard. As minor variations developed from these industry standards, either a new, non−related number was issued by JEDEC or manufacturers would attempt to relate the part to an industry standard via some appended description.

In an attempt to ease confusion, JEDEC established the present system in late 1968 in which new packages are assigned into a category, based on their general physical appearance. Differences between specific packages in a category are denoted by suffix letters. The older package designations were re−registered to the new system as time permitted.

For example the venerable TO−3 has many variations. Can heights differ and it is available with 30, 40, 50, and 60 mil pins, with and without lugs. It is now classified in the TO−204 family. The TO−204AA conforms to the original outline for the TO−3 having 40 mil pins while the TO−204AE has 60 mil pins, for example.

The new numbers for the old parts really haven't caught on very well. It seems that the DO−4, DO−5 and TO−3 still convey sufficient meaning for general verbal communication.

ON Case Number	JEDEC Outline		Notes	Mounting Class
	Original System	Revised System		
001	TO-3	TO-204AA		Flange
003	TO-3		2	Flange
009	TO-61	TO-210AC		Stud
011	TO-3	TO-204AA	–	Flange
011A	TO-3	–	2	Flange
012	TO-3	–	2	Flange
036	TO-60	TO-210AB	–	Stud
042A	DO-5	DO-203AB	–	Stud
044	DO-4	DO-203AA	–	Stud
054	TO-3	–	2	Flange
056	DO-4	–	–	Stud
058	DO-5	–	2	Stud
61-04				Flange
63-02	TO-64	TO-208AB		Stud
63-03	TO-64	TO-2088AB		Stud
077	TO-126	TO-225AA	–	Plastic
080	TO-66	TO-213AA	–	Flange
086	–	TO-208	1	Stud
086L	–	TO-298	1	Stud
144B-05				Stud
145A-09				Stud
145A-10				Stud
145C	TO-232		1	Stud
157	–	DO-203	1	Stud
160-03	TO-59	TO-210AA	–	Stud
167	–	DO-203	1	Stud
174-04				Pressfit

Notes: 1. Would fit within this family outline if registered with JEDEC.
2. Not within all JEDEC dimensions.

ON Case Number	JEDEC Outline		Notes	Mounting Class
	Original System	Revised System		
175-03				Stud
197	–	TO-204AE	–	Flange
211-07				Flange
211-11				Flange
215-02				Flange
221	–	TO-220AB	–	Tab
221C-02				Plastic
221D-02	–	–	Isolated TO-220	Plastic
235	–	TO-208	1	Stud
235-03				Stud
238	–	TO-208	1	Stud
239	–	TO-208	–	Stud
244-04				Stud
245	DO-4	–	–	Stud
257-01	DO-5	–	–	Stud
263	–	TO-208	–	Stud
263-04				Stud
283	DO-4	–	–	Stud
289	–	TO-209	1	Stud
305-01				Stud
310-02				Pressfit
311-02			Isolated	Stud
311-02				Pressfit
311-02				Stud
314B-03				Tab

ON Case Number	JEDEC Outline		Notes	Mounting Class
	Original System	Revised System		
314D-03				Tab
316-01				Flange
319-06				Flange
328A-03				Flange
332-04				Stud
333-04				Flange
333A-02				Flange
336-03				Flange
337-02				Flange
340		TO-218AC		Tab
340A-02				Plastic
340B-03			Isolated TO-218	Plastic
342-01				Flange
357B-01				Flange
361-01				Flange
368-02				Flange
369-06		TO-251		Insertion
369A-12		TO-252		Surface
373-01			Isolated	Flange
383-01			Isolated	Flange
387-01		TO-254AA	Isolated 2	Tab
388A-01		TO-258AA	Isolated 2	Tab
744-02				Flange
744A-01				Flange
043-07	DO-21	DO-208AA		Pressfit

(1) MIL−HANDBOOK − 2178, SECTION 2.2.
(2) “Navy Power Supply Reliability − Design and Manufacturing Guidelines” NAVMAT P4855−1, Dec. 1982 NAVPUBFORCEN, 5801 Tabor Ave., Philadelphia, PA 19120.
(3) Catalog #87−HS−9, (1987), page 8, Thermalloy, Inc., P.O. Box 810839, Dallas, Texas 75381−0839.
(4) ITW Shakeproof, St. Charles Road, Elgin, IL 60120.
(5) Robert Batson, Elliot Fraunglass and James P Moran, “Heat Dissipation Through Thermalloy Conductive Adhesives,” EMTAS ’83. Conference, February 1 − 3, Phoenix, AZ; Society of Manufacturing Engineers, One SME Drive, P.O. Box 930, Dearborn, MI 48128.

AND8081/D

Flip Chip CSP Packages

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ON Semiconductor
Staff Engineer

ON Semiconductor®

http://onsemi.com

APPLICATION NOTE

Introduction to Chip Scale Packaging

This application note provides guidelines for the use of Chip Scale Packages related to mounting devices to a PCB. Included is information on PCB layout for Systems Engineers, and manufacturing processes for Manufacturing Process Engineers.

Package Overview

Flip Chip CSP "Package" Overview

Chip Scale packages offered by ON Semiconductor represent the smallest footprint size since the package is the same size as the die. ON Semiconductor offers two types of CSPs, or bumped die – Flip Chip CSP and Standard Bump. This application note covers only the Flip Chip CSPs with larger bumps.

Flip Chip CSP bumped die are created by attaching 300 μm solder spheres to the I/O pads of the active side of the wafer. The I/O layout can either be peripheral or array. No redistribution layer is used.

The 63/37 SnPb solder bumps allow compatibility of the package connections with standard surface mount technology pick and place and reflow processes and standard flip chip mounting systems. The larger solder bumps of the Flip Chip CSP requires no underfill to increase reliability performance.

Devices designed with the smaller standard bumps generally have a peripheral pad layout and a tighter spacing than that of the Flip Chip CSPs. Underfill is recommended to increase board level solder joint reliability.

Package Construction and Process Description

The Flip Chip CSP is a wafer level processing technique. Upon completion of standard wafer processing, a polymeric BCB passivation layer is applied to the wafer, leaving the bonding pads exposed. A sputtered thin film underbump Al/NiV/Cu metallization (UBM) is applied to the device bonding bonds to provide an interface between the die pad metallization and the solder bump. Solder spheres are placed on each exposed pad and reflowed to create an interconnection system ready for board assembly.

Once the bumps are reflowed, wafers are electrically tested, laser marked, sawn into individual die, and packed in tape and reel, bumps down. A typical Flip Chip CSP is represented in Figure 53. Total device thickness will vary, depending on customer requirements.

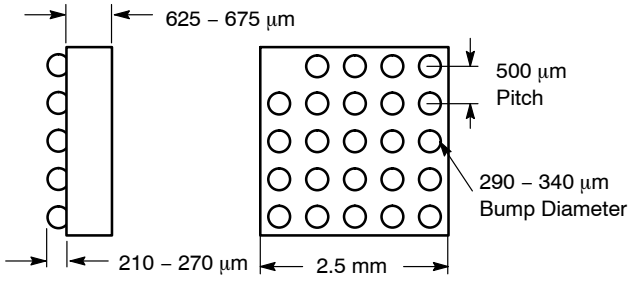

Figure 53. Daisy Chain Flip Chip CSP

Printed Circuit Board Design

Recommended PCB Layout

Two types of land patterns are commonly used for surface mount packages – non−solder mask defined (NSMD) and solder mask defined (SMD), Figure 54. With SMD configured pads, the solder mask covers the outside perimeter of the circular contact pads, thus limiting the solder attach to just the top surface of the exposed pads. With NSMD configured pads, there is a gap between the solder mask and the circular contact pad. NSMD pads are preferred due to better control of the copper etch process as compared with the solder mask etch process in the SMD pad definition. The solder bumps will attach to the NSMD pad wall as well as the pad surface, which provides additional mechanical strength and solder joint fatigue life. SMD pad definition introduces increased levels of stress near the solder mask overlap region which results in solder joint fatigue cracking in extreme temperature cycling conditions. The smaller NSMD pads also provide more room for escape routing on the PCB since they can be smaller in diameter than SMD pads.

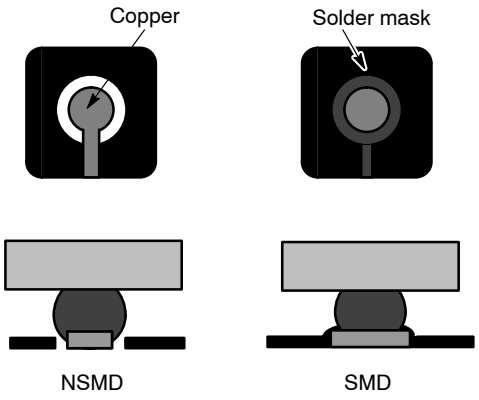

Figure 54. NSMD vs. SMD

A copper layer thickness of less than 1 oz (30 μm) is recommended to maintain a maximum stand−off height and consequently maximum solder joint fatigue life.

Micro−via pads should be NSMD to ensure adequate wetting area of the copper pad.

A summary of recommended design parameters is found in Table 4.

Table 4. PCB Assembly Recommendations

Parameter	500 μm Pitch 300 μm Solder Ball
PCB Pad Size	250 μm $^{+25}_{-0}$
Pad Shape	Round
Pad Type	NSMD
Solder Mask Opening	350 μm ±25
Solder Stencil Thickness	125 μm
Stencil Aperture	250 x 250 μm sq.
Solder Flux Ratio	50/50
Solder Paste Type	No Clean Type 3 or Finer
Trace Finish	OSP Cu
Trace Width	150 μm Max

PCB I/O Contacts Surface Finish Characteristics

Organic solderability preservative (OSP) pad finish is recommended for optimum solder joint reliability. Electroless nickel−immersion gold finish with gold thickness ranging from 0.05 – 0.127 μm may also be used, although solder joint integrity may suffer due to the presence of brittle gold/tin intermetallics. Hot Air Solder Leveled finish (HASL) is not recommended because the process does not give consistent solder volumes on each pad.

Solder Assembly Recommendations

SMT Process Flow

Surface mount assembly operations include printing solder paste onto the PCB.

Solder Paste Characteristics

Type 3 (25 – 45 μm powder), Type 4 (20 – 38 μm powder) or Type 5 (15 – 25 μm powder) ANSI/J−STD−005 compliant solder paste is suggested. No−clean solder paste is recommended. RMA or water soluble (OA) solder paste flux may also be used. Metal load range is from 85 – 90 wt%. Solder flux ratio should be 50/50 by volume.

Solder Stencil and Printing

Stainless steel, brass, or nickel plated stencils with laser cut or metal additive apertures are recommended. Five degree tapered walls are suggested for laser cut stencils to facilitate the release of the paste when the screen is removed from the PCB. Stencil thickness of 0.125 mm with openings approximately the same size as the substrate bond pads are recommended. It is highly recommended that the solder paste height, uniformity, registration and proper placement during the squeegee printing are monitored.

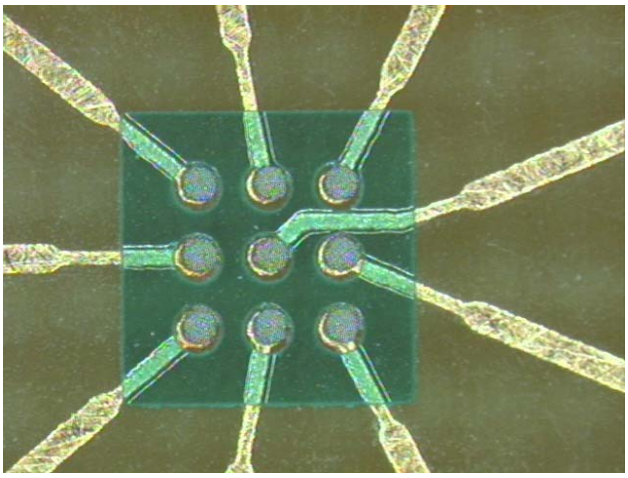

Figure 55. Printed Solder Paste on PCB

Package Placement

Standard pick and place machines can be used for placing CSPs. Such placement equipment falls into two categories: a vision system to locate the package silhouette commonly known as a chip shooter, or a fine pitch vision system to locate individual bumps. It is preferable to use vision systems employing solder sphere recognition for improved placement accuracy, however throughput is reduced. Little or no force should be exerted on the Flip Chip CSP during placement.

Solder Paste Reflow and Cleaning

When cleaning a No−clean or RMA flux residue, semi−aqueous solvents, saponified water, alcohols and other CFC−free alternatives may be used to sufficiently remove all residue. If cleaning a water soluble flux residue, spray and immersion should be sufficient to remove all ionic contamination and residue.

IR Reflow Profile

A standard surface mount reflow process can be used once the part and solder paste or flux are placed on the PCB. An example of a standard reflow profile is shown in Figure 56. The exact recommended reflow profile is determined by the manufacturer of the paste since the chemistry and viscosity of the flux matrix will vary. These variations will require small changes in the profile in order to achieve an optimized process.

In general, for low temperature eutectic SnPb solder, the temperature of the part should be raised less than or equal to 5°C/sec during the initial stages of the reflow profile. The soak zone then occurs when the part is approximately 150°C and should last 30 to 120 seconds. The temperature is then raised and will be above the liquidus of the solder for 30 to 100 seconds depending on the mass of the board. The peak temperature of the profile should be between 225 and 235°C for 10 seconds or less.

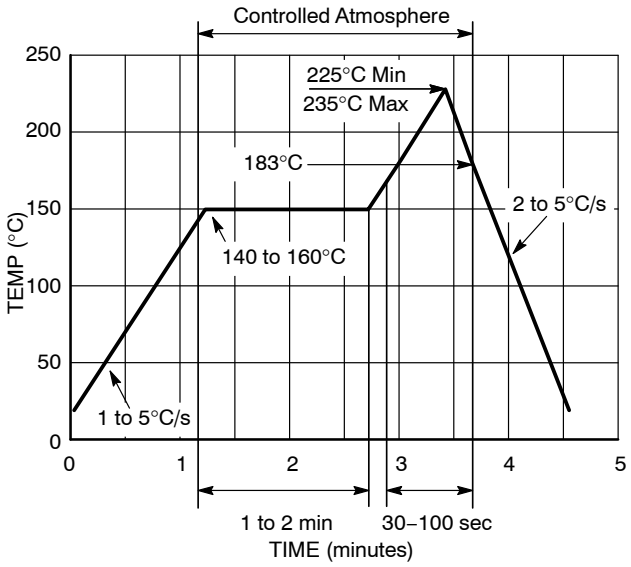

Figure 56. Typical Reflow Profile for Eutectic SnPb Solder

Solder Joint Inspection

The inspection of solder joints is commonly performed with an x−ray inspection system. The x−ray system is used to locate open contacts, shorts between pads, solder voids, and extraneous solder. A cross section of a typical flip chip solder joint is found below in Figure 57.

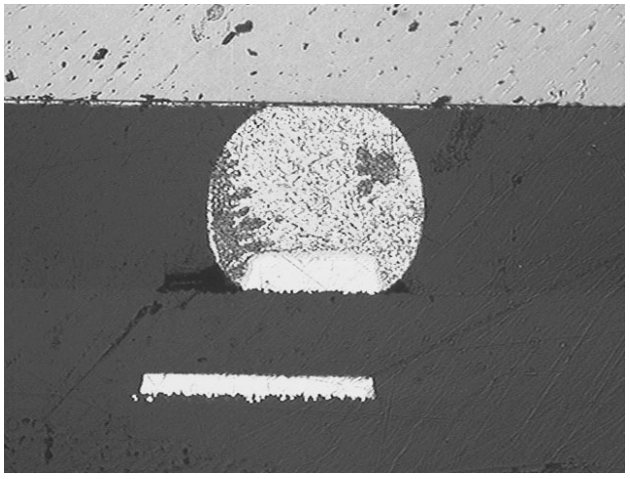

Figure 57. Cross Section of Solder Bump

Underfill

Underfill is not needed for Flip Chip CSP Devices constructed with the larger 300 μm solder spheres. Solder joint reliability tests have shown parts to pass temperature cycling tests without the need for further encapsulation. These devices can, however, withstand the dispense of an underfill as long as the process temperature does not exceed 175°C for up to 5 minutes.

Rework Process

Very similar to that of the rework process for BGAs, the key steps in rework of bumped die product are as follows:

7. CSP removal uses localized heating which duplicates the original reflow profile used for assembly.
8. The reject CSP can be removed once the temperature exceeds the liquidus temperature of the solder.
9. The pads need to be thoroughly cleaned prior to applying flux.
10. A new part is picked up using a vacuum needle pick−up tip and placed onto the board.
11. The replacement part is reflowed to the board using the same convection nozzle and preheat from the bottom, and the original reflow profile.

ON Semiconductor CSP Reliability Test Data

Board Level CSP Package Reliability

ON Semiconductor performed solder joint fatigue testing on Flip Chip CSP test structures per IPC−SM−785 Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments. The test vehicles used were 2.5 x 2.5 mm or 1.5 x 1.5 mm daisy chain die with either a 5 x 5 matrix or a 3 x 3 matrix of solder bumps, respectively, spaced at a pitch of 0.5 mm. These devices were assembled with Type 5 eutectic, SnPb solder paste to .032” thick 4−layer high temperature FR4 test boards, which were designed with 250 μm OSP Cu NSMD pads. Boards were temperature cycled from –40 to 125°C (1 cycle/hr, 15 min ramp, 15 min dwell) and continuously monitored for changes in resistance. The temperature cycling profile is found in Figure 58 below. Table 5 summarizes the daisy chain CSP solder joint reliability test results.

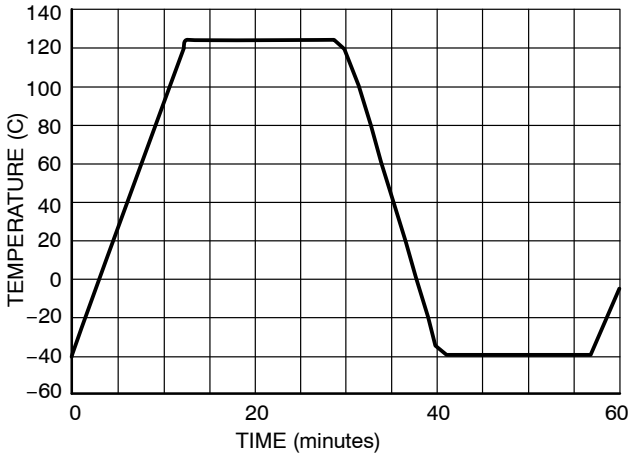

Figure 58. Temperature Cycling Profile for Solder Joint Fatigue Testing

Table 5. ON Semiconductor Flip Chip CSP Solder Joint Reliability Test Results

Flip Chip CSP	Test Condition	Test Board	1210 Cycles	1457 Cycles	1464 Cycles	1643 Cycles
24 bump, 0.32 mm bump diameter	−40 to 125°C, 1 cycle/hr, 15 min ramp, 15 min dwell	OSP Cu pads/flux	0/32	0/32	1/32	3/32
9 bump, 0.32 mm bump diameter	−40 to 125°C, 1 cycle/hr, 15 min ramp, 15 min dwell	NiAu pads/flux	0/32	1/32	1/32	2/32

The test results show that the 1.5 x 1.5 mm CSP devices can pass 1456 temperature cycles, and the 2.5 x 2.5 mm CSP devices can pass 1463 cycles without failure.

Figure 59 is a Weibull plot of the solder joint fatigue data for each of the daisy chain devices.

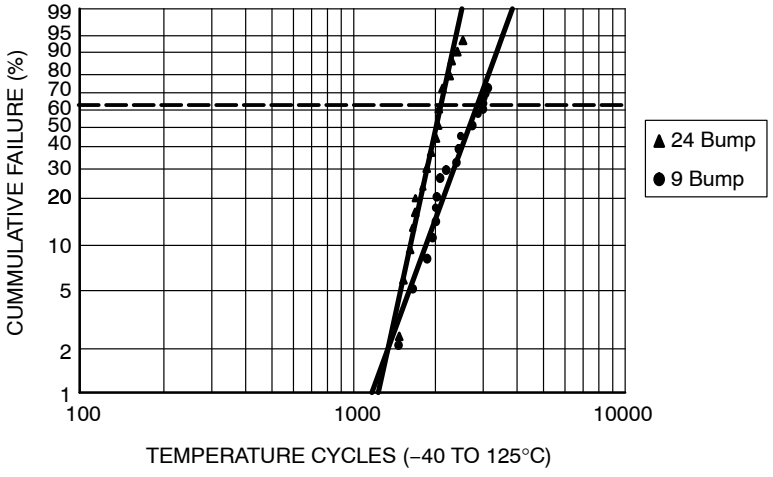

Figure 59. Weibull Plot

Tape and Reel Specifications and Labeling Description

All Flip Chip CSPs are shipped in tape and reel (T & R). CSP T & R requirements are based on the industrial standard EIA−481. The T & R construction is given in Figure 60 below.

Specified tape width: 8 mm

Tape sprocket hole pitch: 4.0 ± 0.1 mm

Compliant to industrial standard EIA−481

The SMD pick and place machines should pick up the component from the point which is located in the center of two adjacent sprocket holes in the feeding direction. This must be taken into account when designing the location of the component in the T & R pocket.

Tape Material:	Small parts other than 0402 (1005 in metric) in 8 mm wide tape: paper (i.e. punched) or embossed (i.e. blister)
Reel Size:	Standard reel diameter is 7 inches (178 mm) for all 8 mm tape.
Reel Material:	Plastic
Device Orientation:	Pin 1 toward sprocket holes.

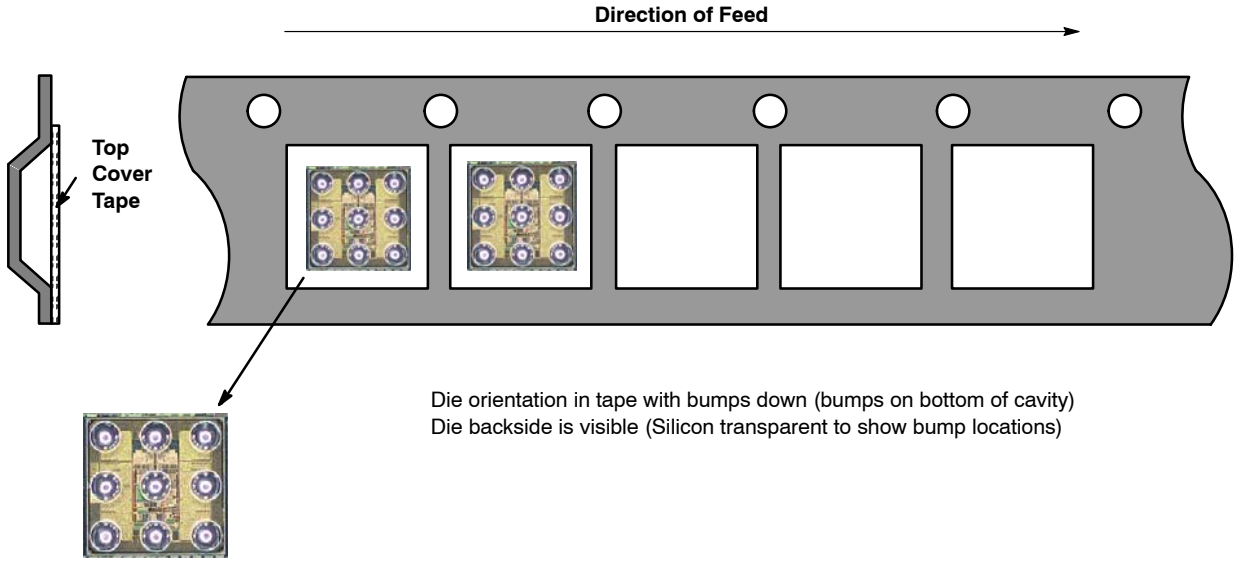

Figure 60. Number of Components per Reel = 3000

The cavity is designed to provide sufficient clearance surrounding the component so that:

1. The part does not protrude beyond either surface of the carrier tape.
2. The part can be removed from the cavity in a vertical direction without mechanical restriction after the top cover tape has been removed.
3. Rotation of the part is limited to 20 degrees maximum.
4. Lateral movement of the part is restricted to 0.05 mm maximum.

Tape with or without parts shall pass around radium R without damage.

Barcode labeling (if required) shall be on the side of the reel opposite the sprocket holes.

(6) Catalog, Edition 18, Richco Plastic Company, 5825 N. Tripp Ave., Chicago, IL 60546.

(7) Herb Fick, “Thermal Management of Surface Mount Power Devices,” Powerconversion and Intelligent Motion, August 1987.

Section 3

Handling of Semiconductor Packages

AND8003/D

Storage and Handling of Drypacked Surface Mounted Devices (SMD)

Prepared by: R. Kampa, D. Hagen, W. Lindsay, and K.C. Brown

ON Semiconductor
Formerly a Division of Motorola
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APPLICATION NOTE

INTRODUCTION

This information provides ON Semiconductor customers with the necessary storage and handling guidelines to preclude component package cracking during solder reflow procedures.

This document applies to plastic encapsulated SMDs that ON Semiconductor identifies as moisture sensitive and delivers in a drypack. Moisture sensitive SMDs include, but are not limited to small outline J pins (SOJs), plastic leaded chip carriers (PLCCs), quad flat packs (QFPs), plastic quad flat packs (PQFPs), thin quad flat packs (TQFPs), thin small outline packages (TSOPs), small outline integrated circuits (SOICs), and plastic ball grid arrays (PBGAs).

SMD PACKAGE LIMITATIONS

During reflow procedures, moisture absorbed from the atmosphere will vaporize inside an SMD and swell into a vapor dome. The internal stresses exerted by the vapor dome are directly proportional to the amount of moisture absorbed prior to reflow. The pressure from the vapor dome may cause of one or more of the internal package interfaces to delaminate. This pressure may also form cracks in the mold compound and possibly expose the die to the external environment.

Both, die surface delaminating and package cracks, pose potential reliability problems. By following the guidelines herein, ON Semiconductor customers will avoid the occurrence of these problems.

DRYPACK DESCRIPTION

Drypack consists of a moisture vapor barrier bag with a preprinted moisture sensitive warning label, a desiccant, and RH indicator, and a barcode label.

The bag construction consists of a three layer laminate; tyvek or nylon for puncture resistance, aluminum for a moisture barrier, and polyethylene for an airtight seal.

The preprinted warning label identifies the contents as moisture sensitive and outlines the recommended storage and handling requirements and shelf life.

The desiccant packed in each bag will keep the internal humidity level below 20% RH for at least one year, under worst case storage conditions of 40°C and 90% RH.

The RH indicator provides the customer with a simple and efficient means to verify that the internal humidity level remains below 20% RH during storage. NOTE: If the RH indicator reads greater than 20% RH at 23°C ± 5°C immediately upon opening the bag, then the SMDs contained therein must undergo a dry−out procedure (see Dry−Out Procedures) prior to any reflow process.

The barcode label identifies the bag seal date and the qualified moisture sensitivity level of the SMD. An ON Semiconductor Standard Operating Procedure (S.O.P.) specification titled “Moisture Characterization and Preconditioning of Plastic Surface Mounted Devices” defines the requirements for qualifying the moisture sensitivity level of a plastic SMD and meets the intent of JEDEC A112, Moisture Induced Stress Sensitivity for Plastic Surface Mounted Devices, and JEDEC A113, Preconditioning of Plastic Surface Mounted Devices Prior to Reliability Testing.

STORAGE REQUIREMENTS AND TIME LIMITS OUT OF DRYPACK

The qualified moisture sensitivity level for each SMD determines the appropriate storage requirements and time limits once out of drypack. Table 6 relates the moisture sensitivity (MS) level to the storage environment and time limits. If these limits are exceeded once the drypack is removed, then the effected SMDs must undergo a dry−out procedure prior to any reflow process.

Table 6.

MS Level	Drypack	Storage TH	Time Out of Drypack
1	No	30°C / 90% RH	Indefinite
2	Yes	30°C / 60% RH	One Year
3	Yes	30°C / 60% RH	168 Hours Max
4	Yes	30°C / 60% RH	72 Hours Max
5	Yes	30°C / 60% RH	24 Hours Max
6	Yes	30°C / 60% RH	6 Hours Max

OPTIONAL STORAGE METHODS OUT OF DRYPACK

If the customer cannot mount the SMDs within the specified time limit, or factory ambient conditions exceed the specified maximum temperature and/or humidity level, then the customer can abate moisture absorption by immediately storing the SMDs at less than 20% RH. Any of the following storage methods may be used.

Store the SMDs in a rigid metal container with a tight fitting lid. Place fresh desiccant (as a minimum, the equivalent of one ON Semiconductor desiccant bag per every 0.8 cubic feet) in the storage container. Desiccant is readily available at any chemical supply house. An RH indicator strip must be kept inside the container to verify that the humidity level remains below 20 percent.

Store the SMDs in a dry nitrogen purge cabinet or container that maintains the humidity level at less than 20 % RH.

For short term storage, SMDs can be resealed in the original drypack bag soon after opening. Bags opened carefully near the seal are easily resealed with either a heat seal or a tight fitting clip. Fresh desiccant may be required in equal proportion to the amount originally shipped with the bag. An RH indicator strip must be kept inside the bag to verify that the humidity level remains below 20% RH.

DRY−OUT PROCEDURES

SMDs that are not handled or stored within specification must undergo one of the following dry−out procedures prior to reflow.

125°C DRY−OUT BAKE

Bake TSOPs at 125°C (± 5°C) for four hours (+1/−0 hour). Bake all other SMDs at 125°C (± 5°C) for eight hours (+1/−0 hour). CAUTION:Do not bake SMDs in shipping trays with a temperature rating of less than 130°C. Do not bake SMDs in plastic tubes or tape and reel (T & R) packaging. Use care in handling SMDs out of their shipping container to maintain lead coplanarity.

40°C DRY−OUT BAKE

Bake TSOPs at 40°C (± 5°C) for 96 hours (± eight hours). Bake all other SMDs at 40°C (± 5°C) for 168 hours (± eight hours). NOTE: This bake is designed for SMDs in plastic tubes or T&R, and is best achieved in a dry nitrogen purge oven. Higher temperatures warp or melt plastic tubes and T&R cover tape separates from carrier tape at 60°C.

ROOM TEMPERATURE DRY−OUT

Store units per Optional Storage Methods for a minimum of 500 hours. This drying method is designed for SMDs in plastic tubes or T&R when a 40°C dry−out bake is not possible or desirable.

NOTE:
The customer must apply the same storage requirements and time limits specified in Storage Requirements to all dried SMDs

SOLDER REFLOW PROFILES

The following guidelines do not necessarily indicate the temperature extremes that can safely be applied to SMDs. In most cases and SMD can withstand higher temperatures than the standard PC board. These guidelines represent good soldering practices that will yield high quality assemblies and minimize rework.

VAPOR PHASE REFLOW

Preheat leads to a nominal temperature of 150°C at a maximum rate of 2°C per second.

Operate the reflow chamber between 215°C and 220°C maximum, with a nominal dwell time of 50 to 80 seconds above the eutectic tin/lead solder melting pint of 183°C. Dwell times should not exceed 120 seconds above the eutectic tin/lead solder melting point of 183°C.

NOTE:
Some vapor phase machines cannot provide preheat, and therefore subject boards and components to rather severe thermal shocks.

INFRARED REFLOW

Preheat leads to a temperature of 100°C minimum and a 140°C maximum rate of 2°C per second.

Generate peak lead temperatures between 205°C minimum and 235°C with a nominal dwell time of 50 to 80 seconds above the eutectic tin/lead solder melting point of 183°C. Dwell times should not exceed 120 seconds above the eutectic tin/lead solder melting point of 183°C.

NOTE:
Peak temperatures can vary greatly across the PC board during IR processes. The variables that contribute to this wide temperature range include the furnace type and the size, mass and relative location of the components on the board. Profiles must be carefully tested to determine the hottest and coolest points on the board. The hottest and coolest points should fall within the recommended temperatures. Thermocouples must be carefully attached directly to the solder joint interface between the package leads and the board with very small amounts of thermally conductive grease or epoxy.

WAVE SOLDER

Preheat leads to a temperature of 100°C minimum and 140°C maximum at a maximum rate of 2°C per second.

Generate a solder wave temperature of 245°C nominal, 265°C maximum, with a nominal dwell time of two to three seconds and a maximum dwell time of five seconds

NOTE:
The wave solder process is suitable for the SOIC, but it is not recommended for PLCC, SOJ, QFP, TSOP, PQFP, TQFP or CQFP because of the high rate of bridging and 0pen solder joints caused by shadowing effects. Thermal shock is much greater if the whole body is immersed in molten solder. Wave solder immersion tests have not been conducted on large PLCC, QFP, PQFP, TQFP and CQFP.

REFERENCE DOCUMENTS

JEDEC Test Method A112, “Moisture Induced Stress Sensitivity for Plastic Surface Mounted Devices.” JEDEC Test Method A113, “Preconditioning of Plastic Surface Mounted Devices Prior to Reliability Testing.” ON Semiconductor S.O.P. titled “Moisture Characterization and Preconditioning of Plastic Surface Mounted Devices.”

MOS Gated Device

HANDLING PRECAUTIONS

All MOS devices have insulated gates that are subject to voltage breakdown. The gate oxide for ON Semiconductor CMOS devices is about 900 Å thick and breaks down at a gate−source potential of about 100 volts. To guard against such a breakdown from static discharge or other voltage transients, the protection networks shown in Figures 1A and 1B are used on each input to the CMOS device.

Static damaged devices behave in various ways, depending on the severity of the damage. The most severely damaged inputs are the easiest to detect because the input has been completely destroyed and is either shorted to V_{DD}, shorted to V_{SS}, or open−circuited. The effect is that the device no longer responds to signals present at the damaged input. Less severe cases are more difficult to detect because they show up as intermittent failures or as degraded performance. Another effect of static damage is that the inputs generally have increased leakage currents.

Although the input protection network does provide a great deal of protection, CMOS devices are not immune to large static voltage discharges that can be generated during handling. For example, static voltages generated by a person walking across a waxed floor have been measured in the 4 −15 kV range (depending on humidity, surface conditions, etc.). Therefore, the following precautions should be observed:

1. Do not exceed the Maximum Ratings specified by the data sheet.
2. All unused device inputs should be connected to V_{DD} or V_{SS}.
3. All low−impedance equipment (pulse generators, etc.) should be connected to CMOS inputs only after the device is powered up. Similarly, this type of equipment should be disconnected before power is turned off.
4. Circuit boards containing CMOS devices are merely extensions of the devices, and the same handling precautions apply. Contacting edge connectors wired directly to device inputs can cause damage. Plastic wrapping should be avoided. When external connections to a PC board are connected to an input of a CMOS device, a resistor should be used in series with the input. This resistor helps limit accidental damage if the PC board is removed and brought into contact with static generating materials. The limiting factor for the series resistor is the added delay. This is caused by the time constant formed by the series resistor and input capacitance. Note that the maximum input rise and fall times should not be exceeded. In Figure 2, two possible networks are shown using a series resistor to reduce ESD (Electrostatic Discharge) damage. For convenience, an equation for added propagation delay and rise time effects due to series resistance size is given.
5. All CMOS devices should be stored or transported in materials that are antistatic. CMOS devices must not be inserted into conventional plastic “snow”, styrofoam, or plastic trays, but should be left in their original container until ready for use.
6. All CMOS devices should be placed on a grounded bench surface and operators should ground themselves prior to handling devices, since a worker can be statically charged with respect to the bench surface. Wrist straps in contact with skin are strongly recommended. See Figure 3 for an example of a typical work station.
7. Nylon or other static generating materials should not come in contact with CMOS devices.
8. If automatic handlers are being used, high levels of static electricity may be generated by the movement of the device, the belts, or the boards. Reduce static build−up by using ionized air blowers or room humidifiers. All parts of machines which come into contact with the top, bottom, or sides of IC packages must be grounded to metal or other conductive material.
9. Cold chambers using CO_2 for cooling should be equipped with baffles, and the CMOS devices must be contained on or in conductive material.
10. When lead−straightening or hand−soldering is necessary, provide ground straps for the apparatus used and be sure that soldering ties are grounded.
11. The following steps should be observed during wave solder operations:
    a. The solder pot and conductive conveyor system of the wave soldering machine must be grounded to an earth ground.
    b. The loading and unloading work benches should have conductive tops which are grounded to an earth ground.
    c. Operators must comply with precautions previously explained.
    d. Completed assemblies should be placed in antistatic containers prior to being moved to subsequent stations.

12. The following steps should be observed during board−cleaning operations:
    a. Vapor degreasers and baskets must be grounded to an earth ground.
    b. Brush or spray cleaning should not be used.
    c. Assemblies should be placed into the vapor degreaser immediately upon removal from the antistatic container.
    d. Cleaned assemblies should be placed in antistatic containers immediately after removal from the cleaning basket.
    e. High velocity air movement or application of solvents and coatings should be employed only when assembled printed circuit boards are grounded and a static eliminator is directed at the board.
13. The use of static detection meters for production line surveillance is highly recommended.
14. Equipment specifications should alert users to the presence of CMOS devices and require familiarization with this specification prior to performing any kind of maintenance or replacement of devices or modules.
15. Do not insert or remove CMOS devices from test sockets with power applied. Check all power supplies to be used for testing devices to be certain there are no voltage transients present.
16. Double check test equipment setup for proper polarity of V_{DD} and V_{SS} before conducting parametric or functional testing.
17. Do not recycle shipping rails or trays. Repeated use causes deterioration of their antistatic coating.

RECOMMENDED FOR READING:

"Total Control of the Static in Your Business"

Available by writing to:
3M Company
Static Control Systems
P.O. Box 2963
Austin, Texas 78769−2963
Or by Calling:
1−800−328−1368

Section 4

Semiconductor Package Reliability and Quality

Semiconductor Package Quality and Reliability

In Brief . . .

The word quality has been used to describe many things, such as fitness for use, customer satisfaction, customer enthusiasm, what the customer says quality is, etc. These descriptions convey important truths, however, quality should be described in a way that precipitates immediate action. With that in mind, quality can be described as reduction of variability around a target, so that conformance to customer requirements and possibly expectations can be achieved in a cost effective way. This definition provides direction and potential for immediate action for a person desiring to improve quality.

The definition of quality as described above can be applied to a task, process or a whole company. If we are to reap the benefits of quality and obtain a competitive advantage, quality must be applied to the whole company.

Implementation of quality ideas company wide requires a quality plan showing: a philosophy (belief) of operation, measurable goals, training of individuals and methods of communicating this philosophy of operation to the whole organization.

ON Semiconductor, for example, believes that quality and reliability are the responsibility of every person. Participative Management is the process by which problem solving and quality improvement are facilitated at all levels of the organization through crossfunctional teams. Continuous improvement for the individual is facilitated by a broad educational program covering onsite, university and college courses. ON Semiconductor University provides leadership and administers this educational effort on a company wide basis.

Another key belief is that quality excellence is accomplished by people doing things right the first time and committed to never ending improvement. The Six Sigma (6σ) challenge is designed to convey and facilitate the idea of continuous improvement at all levels.

The following information provides an overview of the Reliability and Quality principals applicable to semiconductor packaging. For comprehensive information on ON Semiconductor's Reliability and Quality Programs, please refer to Reference Manual R&QARM.

Quality Concepts

Quality improvement for a task or a process can be quickly described in terms of the target, current status with respect to target (variability), reduction of variability (commitment to never ending improvement), customer requirements (who receives output, what are a person's requirements/ expectations) and economics (cost of nonconformance, loss function, etc.).

Application of quality to the whole company has come to be known by such names as **"Total Quality Control" (TQC); "Company Wide Quality Control" (CWQC); "Total Quality Excellence" or "Total Quality Engineering" (TQE); "Total Quality Involvement" (TQI).** These names attempt to convey the idea that quality is a process (a way of acting continuously) rather than a program (implying a beginning and an end). Nevertheless for this process to be successful it must be able to show measurable results.

"**Six Sigma** is the required capability level to approach the standard. The **standard** is **zero defects**. Our goal is to be Best-in-Class in product, sales and service." (For a more detailed explanation, contact your ON Semiconductor Representative for a pamphlet of the Six Sigma Challenge.)

Quick insight into Six Sigma is obtained if we realize that a Six Sigma process has variability which is one half of the variation allowed (tolerance, spread) by the customer requirements (i.e. natural variation is one half of the customer specification range for a given characteristic). When Six Sigma is achieved, virtually zero defects are observed in the output of a process/product even allowing for potential process shifts (Figure 61).

Policies, objectives and five year plans are the mechanisms for communicating the key beliefs and measurable goals to all personnel and continuously keeping them in focus. This is done at the corporate, sector, group, division, and department levels.

ON Semiconductor, for example, evaluates performance to the corporate goals of **10 fold improvement by 1989; 100 fold improvement by 1991** and achievement of **Six Sigma capability by 1992** by utilizing indices such as Outgoing Electrical and Visual Mechanical Quality **(AOQ)** in terms of PPM (parts per million or sometimes given in parts per billion); **% of devices with zero PPM ; product quality returns** (RMR); number of processes/products with specified **capability indices (cp, cpk); Six Sigma capability roadmaps; failure rates for various reliability tests** (operating life, temperature humidity bias, hast, temperature cycling, etc.); **on-time delivery; customer product evaluation and failure analysis turnaround; cost of nonconformance; productivity improvement and personnel development**.

Figure 62 shows the improvement in electrical outgoing quality for analog products over recent years in a normalized form. Figure 63 shows the number of parts with zero PPM over a period of time.

Documentation control is an important part of **statistical process control. Process mapping** (flow charting etc.) with documentation identified allows visualization and therefore optimization of the process. Figure 64 shows a portion of a flow chart for wafer fabrication. **Control plans** are an important part of Statistical Process Control, these plans identify in detail critical points where data for process control is taken, parameters measured, frequency of measurements, type of control device used, measuring equipment, responsibilities and reaction plans. Figure 65 shows a portion of a control plan for wafer fabrication. Six Sigma progress is tracked by roadmaps based on the Six Sigma process, a portion of which is shown on Figure 66.

On-time delivery is of great importance, with the current emphasis on **just-in-time** systems. Tracking is done on an overall basis, and at the device levels.

Figure 61. A Six Sigma Process Has Virtually Zero Defects Allowing for 1.5σ Shift

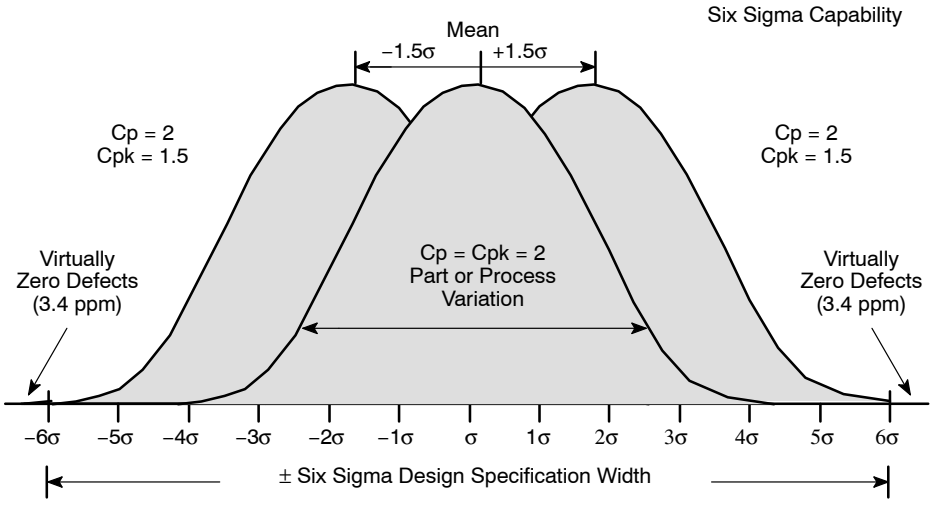


Figure 62. ON Semiconductor Logic & Analog Technologies Group Electrical AOQ

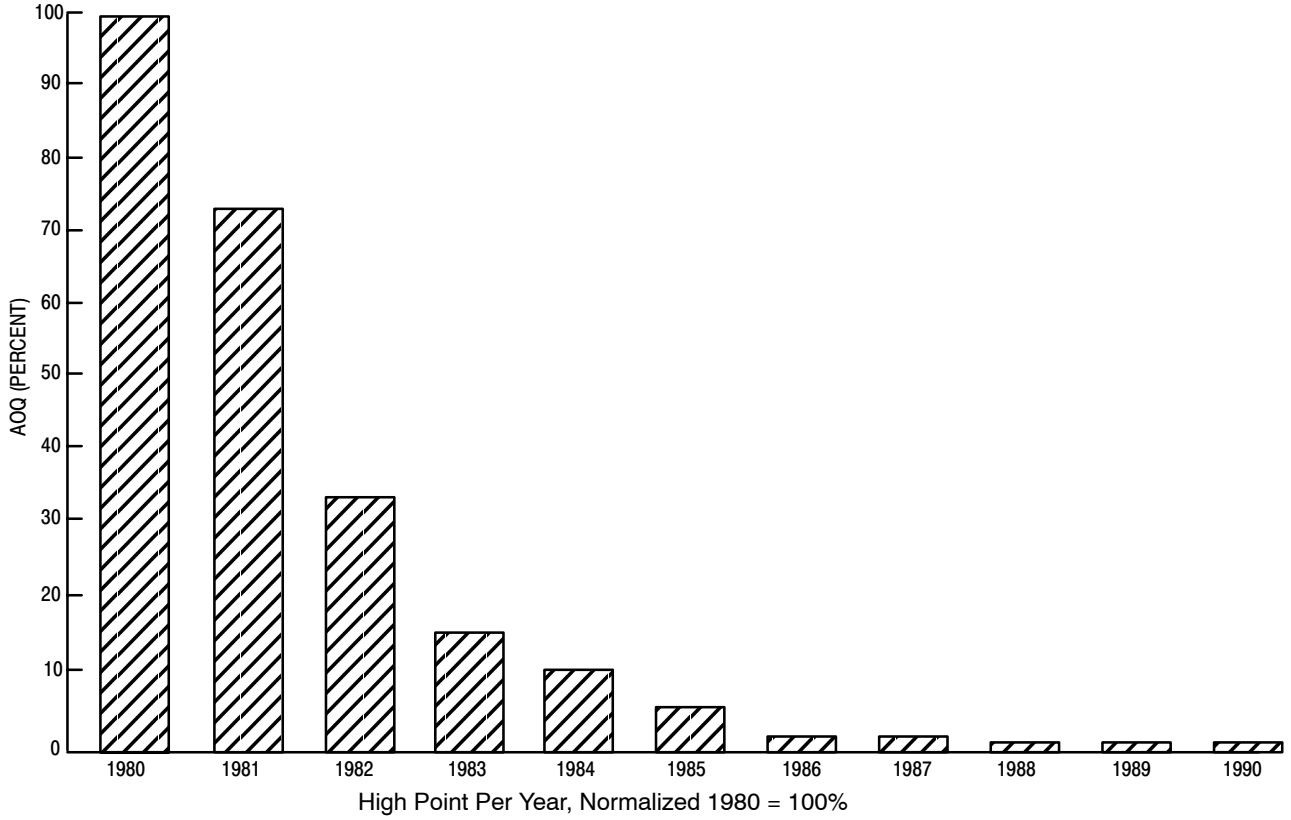


Figure 63. Percentage of Parts with Zero PPM AOQ

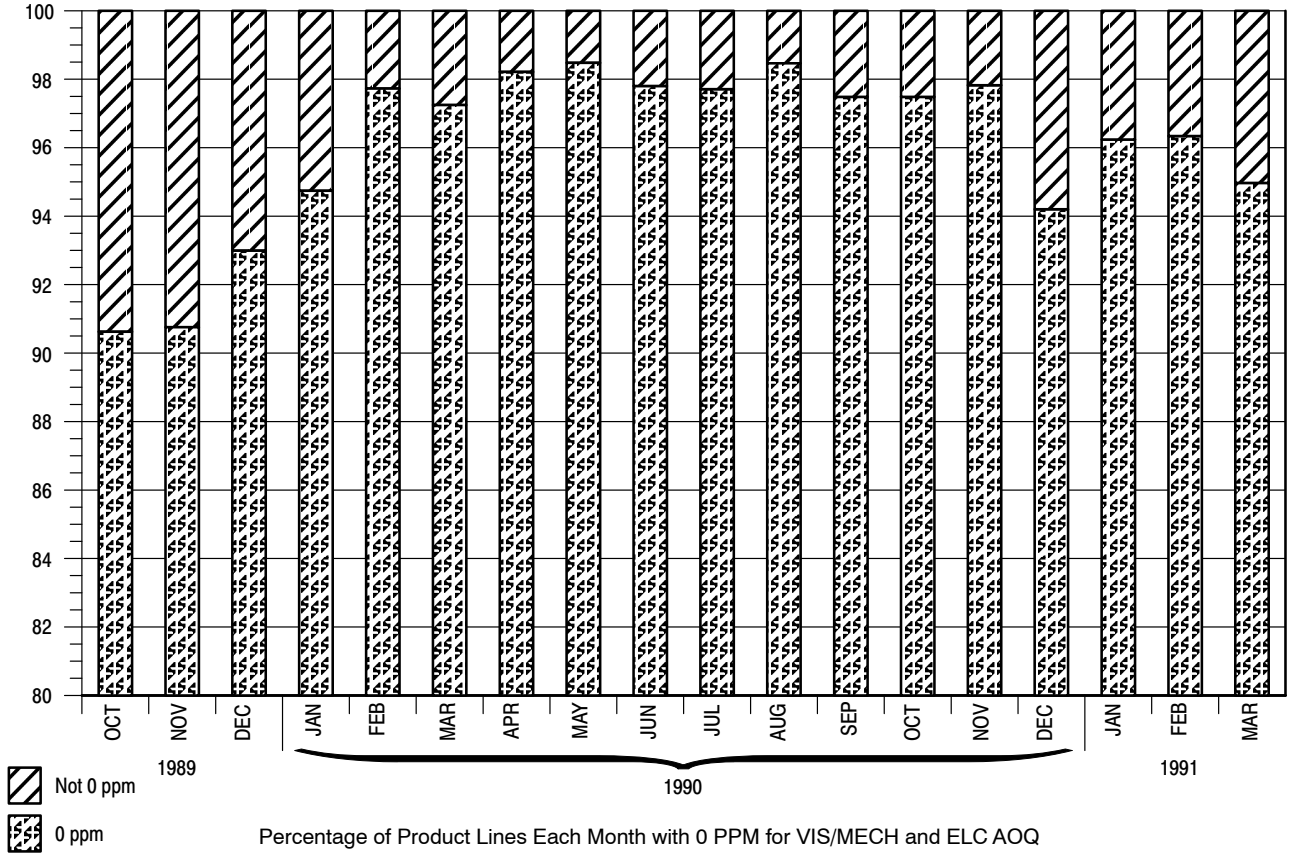


Figure 64. Portion of a Process Flow Chart From Wafer Fab, Showing Documentation Control and SPC

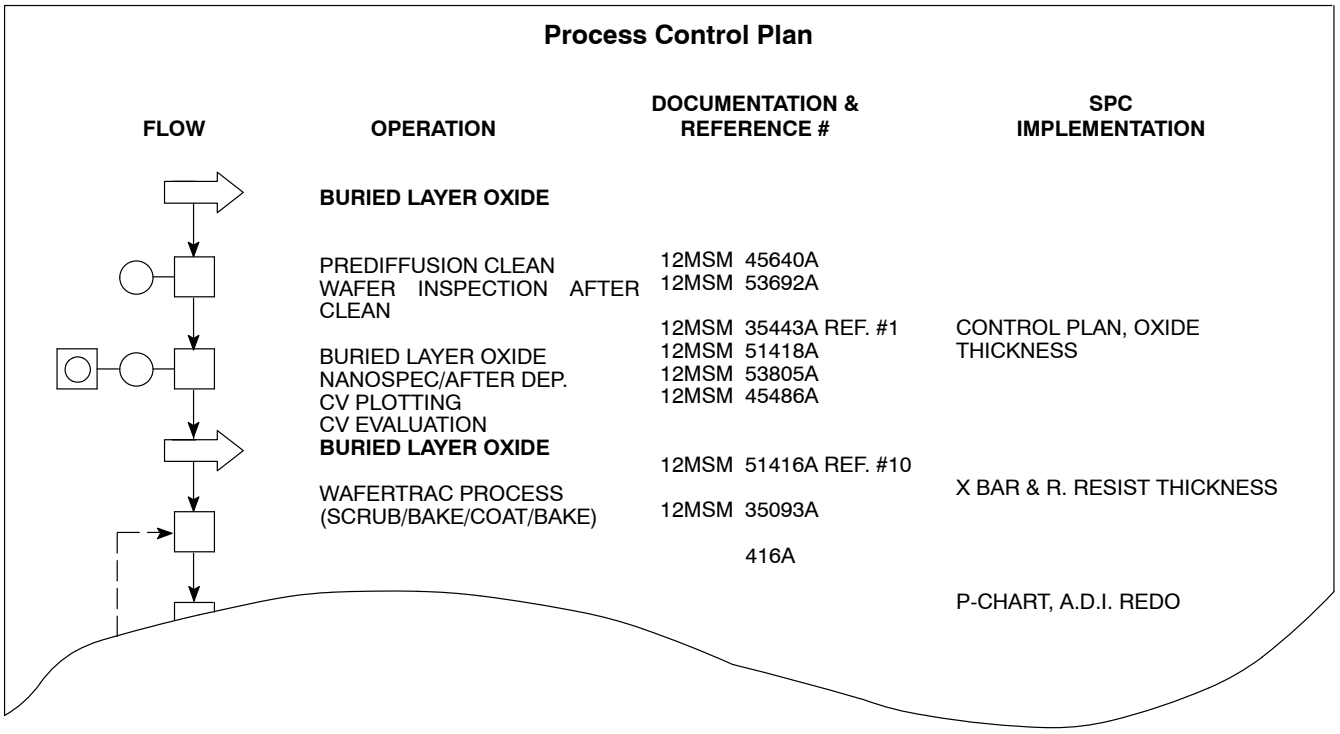


Figure 65. Part of a Wafer Fab Control Plan, Showing Statistical Process Control Details

Characteristics:	Code	Description	Code	Description
	A	VISUAL DEFECTS	E	FILM SHEET RESISTANCE
	B	VISUAL DEFECTS . . . MICROSCOPE	F	REFRACTIVE INDEX
	C	PARTICLE . . . MONITOR	G	CRITICAL DIMENSION
	D	FILM THICKNESS	H	CV PLOT

Process Location	Ref. No.	Characteristic Affected	Part/Process Detail	Measurements Method	Analysis Methods	Frequency Sample Size	Reaction Plan: Point out of Limit (3) (4)
B.L. OXIDE	1	D	OXIDE THICKNESS	NANOMETRIC	CONTROL GRAPH	EVERY RUN 3 WFR/RUN	IMPOUND LOT (1) ADJUST TIME TO CENTER PROCESS PER SPEC
EPI	2	D	THICKNESS	DIGILAB	$\overline{X}$ R CHART	EVERY RUN 5 SITES/WFR	IMPOUND LOT (1) NOTIFY ENGR.
QA		D	THICKNESS	DIGILAB	$\overline{X}$ R CHART	1WFR/SHIFT 5 SITES/WFR	IMPOUND LOT (2) NOTIFY ENGR.
		E	FILM RESISTIVITY	4PT PROBE	$\overline{X}$ R CHART	EVERY RUN 5 SITES/WFR	IMPOUND LOT (1) NOTIFY ENGR.
QA		E	FILM RESISTIVITY	4PT PROBE	$\overline{X}$ R CHART	1WFR/SHIFT 5 SITES/WFR	IMPOUND LOT (2) NOTIFY ENGR.
DEEP				4PT PROBE	MOVING R	EVERY LOT 1 CTRL WFR PER LOT	IMPOUND LOT NOTIFY ENGR.

Figure 66. Portion of Six Sigma (6σ) Roadmap Showing Steps to Six Sigma Capability

STEP	±6σ Summary
1. Identify critical characteristics	• Product Description • Marketing • Industrial Design • R&D/Developmental Engineering • Actual or Potential Customers
2. Determine specified product elements contributing to critical characteristics	• Critical Characteristics Matrix • Cause-and-Effect and Ishikawa Diagrams • Success Tree/Fault Tree Analysis • Component Search or Other Forms of Planned Experimentation • FMECA (Failure Mode Effects and Critical Analysis)
3. For each product element, determine the process step or process choice that affects or controls required performance	• Planned Experiments • Computer-Aided Simulation • TOP/Process Engineering Studies • Multi-Vari Analysis • Comparative Experiments
4. Determine maximum (real) allowable tolerance for each and process	• Graphing Techniques • Engineering Handbooks • Planned Experiments • Optimization, Especially Response Surface Methodology

Reliability Concepts

Reliability is the probability that an analog integrated circuit will successfully perform its specified function in a given environment for a specified period of time. This is the classical definition of reliability applied to analog integrated circuits.

Another way of thinking about reliability is in relationship to quality. While **quality** is a measure of variability (extending to potential nonconformances-rejects) in the population domain, **reliability** is a measure of variability (extending to potential nonconformances-failures) in the population, time and environmental conditions domain. In brief, **reliability** can be thought of as **quality over time** and **environmental conditions**.

Ultimately, **product reliability** is a function of proper **understanding** of **customer requirements** and **communicating** them throughout design, product/process development, manufacturing and final product use. **Quality Function Deployment (QFD)** is a technique which may be used to facilitate identification of customer quality and reliability requirements and communicating them throughout an organization.

The most frequently used reliability measure for integrated circuits is the **failure rate expressed** in percent per thousand device hours (%/1000 hrs.). If the time interval is small the failure rate is called **Instantaneous Failure Rate** [λ (t)] or "Hazard Rate." If the time interval is long (for example total operational time) the failure rate is called **Cumulative Failure Rate**.

The number of failures observed, taken over the number of device hours accumulated at the end of the observation period and expressed as a percent is called the point estimate failure rate. This however, is a number obtained from observations from a sample of all integrated circuits. If we are to use this number to estimate the failure rate of all integrated circuits (total population), we need to say something about the risk we are taking by using this estimate. A **risk** statement is provided by the **confidence level** expressed together with the failure rate. Mathematically, the failure rate at a given confidence level is obtained from the point estimate and the **CHI square** (X^2) distribution. (The X^2 is a statistical distribution used to relate the observed and expected frequencies of an event.) In

practice, a reliability calculator rule is used which gives the failure rate at the confidence level desired for the number of failures and device hours under question.

As the number of device hours increases, our confidence in the estimate increases. In integrated circuits, it is preferred to make estimates on the basis of failures per 1,000,000,000 (10^9) device hours **(FITS)** or more. If such large numbers of device hours are not available for a particular device, then the point estimate is obtained by pooling the data from devices that are similar in process, voltage, construction, design, etc., and for which we expect to see the same failure modes in the field.

The environment is specified in terms of the temperature, electric field, relative humidity, etc., by an **Eyring** type equation of the form:

$$\lambda = Ae^{-\frac{\phi}{KT}} \ldots e^{-\frac{B}{RH}} \ldots e^{-\frac{C}{E}}$$

where A, B, C, ϕ & K are constants, T is temperature, RH is relative humidity, E is the electric field, etc.

The most familiar form of this equation deals with the first exponential which shows an **Arrhenius type** relationship of the **failure rate** versus the **junction temperature** of integrated circuits, while the causes of failure generally remain the same. Thus we can test devices near their maximum junction temperatures, analyze the failures to assure that they are the types that are accelerated by temperature and then applying known acceleration factors, estimate the failure rates for lower junction temperatures. The Eyring or Arrhenius relationships should be used for failure rate projections in conjunction with proper understanding of failure modes, mechanisms and patterns such as infant mortality, constant failure rate (useful region) and wearout. For example if by design and proper process control infant mortality and useful period failures have been brought to zero and wearout failures do not start until, let us say, 30,000 hours at 125°C then failure rate projections at lower temperatures must account for these facts and whether the observed wearout failures occur at lower temperatures.

Figure 67 shows an example of a curve which gives estimates of failure rates versus temperature for an integrated circuit case study.

Arrhenius type of equation: $\lambda = Ae^{-\frac{\phi}{KT}}$

where:
- λ = Failure Rate
- A = Constant
- e = 2.72
- ϕ = Activation Energy
- K = Botzman's Constant
- T = Temperature in Degrees Kelvin

$T_J = T_A + \theta_{JA} P_D$ or $T_J = T_C + \theta_{JC} P_D$

where:
- T_J = Junction Temperature
- T_A = Ambient Temperature
- T_C = Case Temperature
- θ_{JA} = Junction to Ambient Thermal Resistance
- θ_{JC} = Junction to Case Thermal Resistance
- P_D = Power Dissipation

Life patterns (failure rate curves) for equipment and devices can be represented by an idealized graph called the **Bathtub Curve** (Figure 68).

There are three important regions identified on this curve. In Region A, the failure rate decreases with time and it is generally called **infant mortality** or early life failure region. In Region B, the failure rate has reached a relatively constant level and it is called **constant failure rate** or useful life region**.** In the third region, the failure rate increases again and it is called **wearout region**. Modern integrated circuits generally do not reach the wearout portion of the curve when operating under normal use conditions.

Figure 67. Example of a Failure Rate versus Junction Temperature Curve

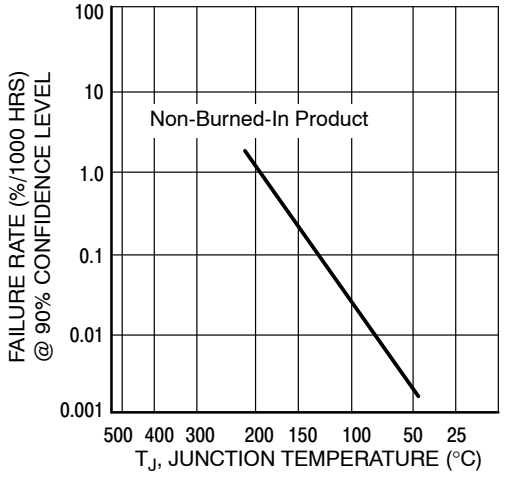
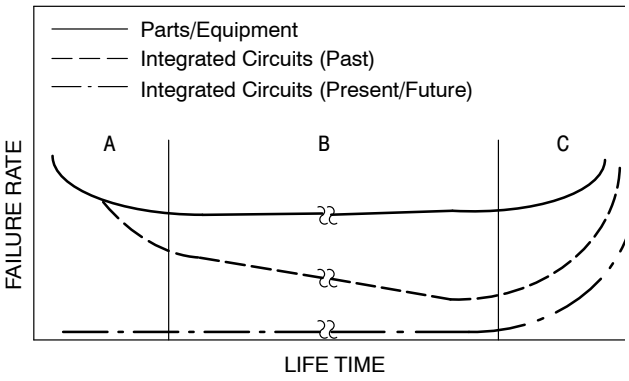


Figure 68. A Model for Failure Distribution in Time Domain Bathtub Curve Model



Decreasing Failure Rate	Constant Failure Rate	Increasing Failure Rate
Infant Mortality Burn-In Manufacturing Variations Workmanship Defects	Useful Life Random (Chance) Defects (No Pattern; Occur Regularly)	Wearout Material, Design, Process Limitations
Weibull Log Normal Gamma Distribution	Weibull Exponential for Equipment Log Normal for ICs	Weibull Normal (Gaussian)

The wearout portion of the curve can usually be identified by using highly accelerated test conditions. For modern integrated circuits, even the useful life portion of the curve may be characterized by few or no failures. As a result the bathtub

curve looks like continuously declining (few failures, Figure 68, Curve B) or zero infant and useful period failures (constant failure rate until wearout, Curve C).

The **infant mortality** portion of the curve is of most interest to equipment manufacturers because of its impact on customer perception and potential warranty costs. In recent years the infant mortality portion of the curve for integrated circuits, and even equipment, has been drastically reduced

(Figure 68, Curve C). The reduction was accomplished by improvements in technology, emphasis on statistical process control, reliability modeling in design and reliability in manufacturing (wafer level reliability, assembly level reliability, etc.). In this respect many integrated circuit families have zero or near zero failure patterns until wearout starts.

Does a user still need to consider burn-in? For this question to be answered properly the IC user must consider the **target failure rate** of the equipment, **apportioned** to the components used, application environment, maturity of equipment and components (new versus mature technology), the impact of a failure (i.e. safety versus casual loss of entertainment), maintenance costs, etc. Therefore, if the IC user is going through these considerations for the first time, the question of burn-in at the component level should be discussed during a user-vendor interface meeting.

A frequently asked question is about the reliability differences between **plastic** and **hermetic** packaged integrated circuits. In general, for all integrated circuits including analog, the field removal rates are the same for normal use environments, with many claims of plastic being better because of its ‘‘solid block” structure.

The tremendous decrease of failure rates of plastic packages has been accomplished by **continuous improvements** in piece parts, materials and processes. Nevertheless, differences can still be observed under highly accelerated environmental stress conditions. For example, if a bimetallic (gold wire and aluminum metallization) system is used in plastic packages and they are placed on a high temperature operating life test (125°C) then failures in the form of opens, at the gold to aluminum interface, may not be observed until 30,000 hours of continuous operating life. Packages, whether plastic or hermetic, with a monometallic system (aluminum wire to aluminum metallization) will have no opens because of the absence of the gold to aluminum interface. As a result, a difference in failure rates will be observable.

Differences in failure rates between plastics and hermetics may also be observed if devices from both packaging systems are placed in a moist environment such as 85°C, 85% RH with bias applied. At some point in time plastic encapsulated ICs should fail since they are considered pervious by moisture, (the failure mechanism being corrosion of the aluminum metallization) while hermetic packages should not fail since they are considered impervious by moisture. The reason the word ‘‘should” was used is because advances in plastic compounds, package piece parts, encapsulation processes and final chip passivation have made plastic integrated circuits capable of operating more than 5000 hours without failures in an 85°C, 85% RH environment. Differences in failure rates due to internal corrosion between plastic and hermetic packages may not be observable until well after 5000 operating hours.

The aforementioned two examples had environments substantially more accelerated than normal life so the two issues discussed are not even a factor under normal use conditions. In addition, mechanisms inherent in hermetic packages but absent in plastics were not even considered here. Improved reliability of plastic encapsulated ICs has decreased demand of hermetic packages to the point where many devices are offered only in plastic packages. The user then should feel comfortable in using the present plastic packaging systems.

A final question that is asked by the IC user is, how can one be assured that the reliability of standard product does not degrade over time? This is accomplished by our emphasis on **statistical process control, in-line reliability** assessment and **reliability auditing** by periodic and strategic sampling and accelerated testing of the various integrated circuit device packaging systems. A description of these audit programs follows.

ON Semiconductor Reliability Audit Program

The reliability of a product is a function of proper understanding of the application and environmental conditions that the product will encounter during its life as well as design, manufacturing process and final use conditions. **Inherent reliability** is the reliability which a product would have if there were no imperfections in the materials, piece parts and manufacturing processes of the product. The presence of imperfections gives rise to reliability risks. **Failure Mode and Effects Analysis (FMEA)** is a technique for identifying, controlling and eliminating potential failures from the design and manufacture of the product.

ON Semiconductor uses **on-line** and **off-line** reliability monitoring in an attempt to prevent situations which could degrade reliability. **On-line** reliability monitoring is at the **wafer and assembly levels** while **off-line** reliability monitoring involves reliability assessment of the **finished product** through the use of **accelerated** environmental tests.

Continuous monitoring of the reliability of analog integrated circuits is accomplished by the **Analog Reliability Audit Program**, which is designed to compare the actual reliability to that specified. This objective is accomplished by periodic and strategic sampling of the various integrated circuit device packaging systems. The samples are tested by subjecting them to accelerated environmental conditions and the results are reviewed for unfavorable trends that would indicate a degradation of the reliability or quality of a particular packaging system. This provides the trigger mechanism for initiating an investigation for **root cause** and **corrective action**. Concurrently, in order to provide a minimum of interruption of product flow and assure that the product is fit for use, a lot by lot sampling or a non-destructive type 100% screen may be used to assure that a particular packaging system released for shipment does have the expected reliability. This rigorous surveillance is continued until there is sufficient proof (many consecutive lots) that the problem has been corrected.

The **Logic and Analog Technologies Group** has used reliability audits since the late sixties. Such programs have been identified by acronyms such as CRP (Consumer Reliability Program), EPIIC (Environmental Package Indicators for Integrated Circuits), LAPP (Linear Accelerated Punishment Program), and RAP (Reliability Audit Program).

Currently, the Analog Reliability Audit Program consists of a **Weekly Reliability Audit** and a **Quarterly Reliability Audit**. The Weekly Reliability Audit consists of rapid (short time) types of tests used to monitor the production lines on a real time basis. This type of testing is performed at the assembly/test sites worldwide. It provides data for use as an **early warning system** for identifying negative trends and triggering investigations for root cause and corrective actions.

The Quarterly Reliability Audit consists of long term types of tests and is performed at th U.S. Bipolar Analog Division Center. The data obtained from the Quarterly Reliability Audit is used to assure that the correlation between the short term weekly tests and long term quarterly tests has not changed and a new failure mechanism has not appeared.

A large data base is established by combining the results from the Weekly Reliability Audit with the results from the Quarterly Reliability Audit. Such a data base is necessary for estimating long term failure rates and evaluating potential process improvement changes. Also, after a process improvement change has been implemented, the Analog Reliability Audit Program provides a system for monitoring the change and the past history data base for evaluating the affect of the change.

Weekly Reliability Audit

The Weekly Reliability Audit is performed by each assembly/test site worldwide. The site must have capability for final electrical and quality assurance testing, reliability testing and first level of failure analysis. The results are reviewed on a continuous basis and corrective action is taken when appropriate. The results are accumulated on a monthly basis and published.

The Reliability Audit test plan is as follows:

Electrical Measurements: Performed initially and after each reliability test, consist of critical parameters and functional testing at 25°C on a go-no-go basis.

High Temperature Operating Life: Performed to detect failure mechanisms that are accelerated by a combination of temperature and electric fields. Procedure and conditions are per MIL-STD-883, Method 1015 with an ambient temperature of 145°C for 40 hours or equivalent based on a 1.0 eV activation energy and the Arrhenius equation.

Approximate Accelerated Factors

	125°C	50°C
145°C	4	4000
125°C	1	1000

Temperature Cycling/Thermal Shock: Performed to detect mechanisms related to thermal expansion and contraction of dissimilar materials, etc. Procedures and conditions are per MIL-STD-883, Methods 1010 or 1011, with ambient temperatures of −65° to +150°C or −40° to +125°C (JEDEC-STD-22-A104), for a minimum of 100 cycles.

Pressure Temperature Humidity (Autoclave): Performed to measure the moisture resistance of plastic encapsulated packages. It detects corrosion type failure mechanisms due to free ionic contaminants that may have entered the package during the manufacturing processes.

Conditions are per JEDEC-STD-22, Method 102, a temperature of 121°C, steam environment and 15 psig. The duration of the test is 96 hours (minimum).

Analysis Procedure: Devices failing to meet the electrical criteria after being subjected to an accelerated environment type test are verified and characterized electrically, then submitted for failure analysis.

Quarterly Reliability Audit

The Quarterly Analog Reliability Audit Program is performed at the U.S. Bipolar Analog Division Center. This testing is designed to assure that the correlation between the short term weekly tests and the longer quarterly tests has not changed and that no new failure mechanisms have appeared. It also provides additional long term information for a data base for estimating failure rates and evaluation of potential process improvement changes.

Electrical Measurements: Performed initially and at interim readouts, consist of all standard DC and functional parameters at 25°C, measured on a go-no-go basis.

High Temperature Operating Life Test: Performed to detect failure mechanisms that are accelerated by a combination of temperature and electric fields. Procedure and conditions are per MIL-STD-883, Method 1015, with an ambient temperature of 145°C for 40 and 250 hours or equivalent, based on 1.0 eV activation energy and the Arrhenius equation.

Approximate Accelerated Factors

	125°C	50°C
145°C	4	4000
125°C	1	1000

Temperature Cycling/Thermal Shock: Performed to detect mechanisms related to thermal expansion and contraction, mismatch effects, etc. Procedure and conditions are per MIL-STD-883, Methods 1010 or 1011, with ambient temperatures of −65° to +150°C or −40° to +125°C (JEDEC-STD-22-A104) for 100, 500 and 1000 or more cycles, depending on the temperature range used. Temperature Cycling is used more frequently than Thermal Shock.

Pressure Temperature Humidity (Autoclave): Performed to measure the moisture resistance of plastic encapsulated packages. It detects corrosion type failure mechanisms due to free ionic contaminants that may have entered the package during the manufacturing processes. Conditions are per JEDEC-STD-22, Method 102, a temperature of 121°C, steam environment and 15 psig. The duration of the test is for 96 hours (minimum), with a 48 hour interim readout.

Pressure Temperature Humidity Bias (PTHB; Biased Autoclaved): This test measures the moisture resistance of plastic encapsulated packages. It detects corrosion type failure mechanisms due to free and bounded ionic contaminants that may have entered the package during the manufacturing processes, or they may be bound in the materials of the integrated circuit packaging system and activated by the moisture and the applied electrical fields. Conditions are per JEDEC-STD-22, Method 102, with bias applied, a temperature of 121°C, steam environment and 15 psig. This test detects the same type of failures as the Temperature Humidity Bias (85°C, 85% RH, with bias) test, only faster. The acceleration factor between PTHB and THB is between 20 and 40 times, depending on the type of corrosion mechanism, electrical field and packaging system.

Highly Accelerated Stress Test (HAST) is increasingly replacing the aforementioned **PTHB** test. The reason is that the **HAST** test allows control of pressure, temperature and humidity independently of each other, thus we are able to set different combinations of temperature and relative humidity. The most frequently used combination is **130°C with 85% RH**. This has been related to THB (85°C, 85% RH) by an **acceleration factor of 20** (minimum). The ability to keep the relative humidity variable constant for different temperatures is the most appealing factor of the HAST test because it reduces the determination of the acceleration factor to a single Arrhenius type of relationship. ON Semiconductor has been phasing over to HAST testing since 1985.

Temperature, Humidity and Bias (THB): This test measures the moisture resistance of plastic encapsulated packages. It detects corrosion type failure mechanisms due to free and bounded ionic contaminants that may have entered the package during the manufacturing processes, or they may be bound in the materials of the integrated circuit packaging system and activated by moisture and the applied electrical fields. Conditions are per JEDEC-STD-22, Method 102 (85°C, 85% RH), with bias applied. The duration is for 1008 hours, with a 504 hour interim readout. The acceleration factor between THB (85°C, 85% RH with bias) and the 30°C, 90% RH is typically 40 to 50 times, depending on the type of corrosion mechanism, electrical field and packaging system.

Analysis Procedure: Devices failing to meet the electrical criteria after being subjected to an accelerated environment type test(s) are verified and characterized electrically, then they are submitted for root cause failure analysis and corrective action for continuous improvement.

OPTIMIZING THE LONG TERM RELIABILITY OF PLASTIC PACKAGES

Todays plastic integrated circuit packages are as reliable as ceramic packages under most environmental conditions. However when the ultimate in system reliability is required, thermal management must be considered as a prime system design goal.

Modern plastic package assembly technology utilizes gold wire bonded to aluminum bonding pads throughout the electronics industry. When exposed to high temperatures for protracted periods of time an intermetallic compound can form in the bond area resulting in high impedance contacts and degradation of device performance. Since the formation of intermetallic compounds is directly related to device junction temperature, it is incumbent on the designer to determine that the device junction temperatures are consistent with system reliability goals.

Predicting Bond Failure Time:

Based on the results of almost ten (10) years of +125°C operating life testing, a special arrhenius equation has been developed to show the relationship between junction temperature and reliability.

$$\text{Eq. (1) } T = (6.376 \times 10^{9})e\left[\frac{11554.267}{273.15 + T_J}\right]$$

Where: T = Time in hours to 0.1% bond failure (1 failure per 1,000 bonds).

T_J = Device junction temperature, °C.

And:

$$\text{Eq. (2) } T_J = T_A + P_D\theta_{JA} = T_A + \Delta T_J$$

Where: T_J = Device junction temperature, °C.

T_A = Ambient temperature, °C.

P_D = Device power dissipation in watts.

θ_{JA} = Device thermal resistance, junction to air, °C/Watt.

ΔT_J = Increase in junction temperature due to on−chip power dissipation.

Table 7 shows the relationship between junction temperature, and continuous operating time to 0.1%. bond failure, (1 failure per 1,000 bonds).

Table 7. Device Junction Temperature versus Time to 0.1% Bond Failures

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

Table 7 is graphically illustrated in Figure 67 which shows that the reliability for plastic and ceramic devices are the same until elevated junction temperatures induces intermetallic failures in plastic devices. Early and mid−life failure rates of plastic devices are not effected by this intermetallic mechanism.

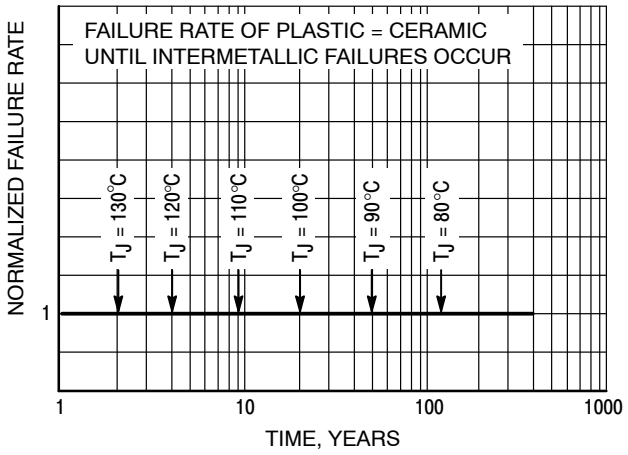


Figure 69. Failure Rate versus Time Junction Temperature

Procedure

After the desired system failure rate has been established for failure mechanisms other than intermetallics, each device in the system should be evaluated for maximum junction temperature. Knowing the maximum junction temperature, refer to Table 7 or Equation 1 to determine the continuous operating time required to 0.1% bond failures due to intermetallic formation. At this time, system reliability departs from the desired value as indicated in Figure 67.

Air flow is one method of thermal management which should be considered for system longevity. Other commonly used methods include heat sinks for higher powered devices, refrigerated air flow and lower density board stuffing. Since $\overline{\theta}_{CA}$ is entirely dependent on the application, it is the responsibility of the designer to determine its value. This can be achieved by various techniques including simulation, modeling, actual measurement, etc.

The material presented here emphasizes the need to consider thermal management as an integral part of system design and also the tools to determine if the management methods being considered are adequate to produce the desired system reliability.

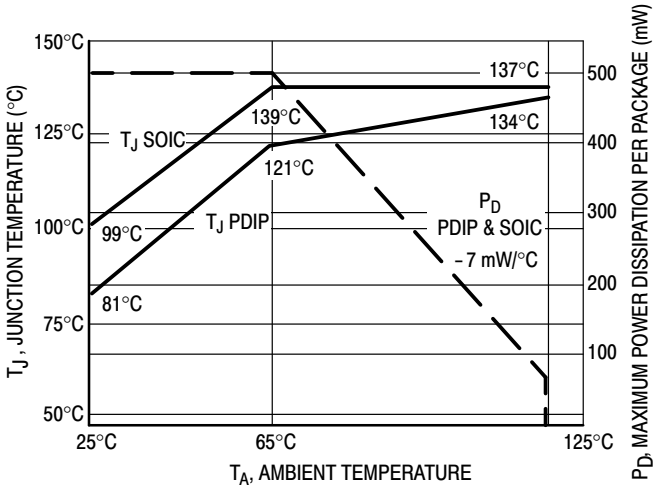


Figure 70. Junction Temperature for Worst Case CMOS Logic Device

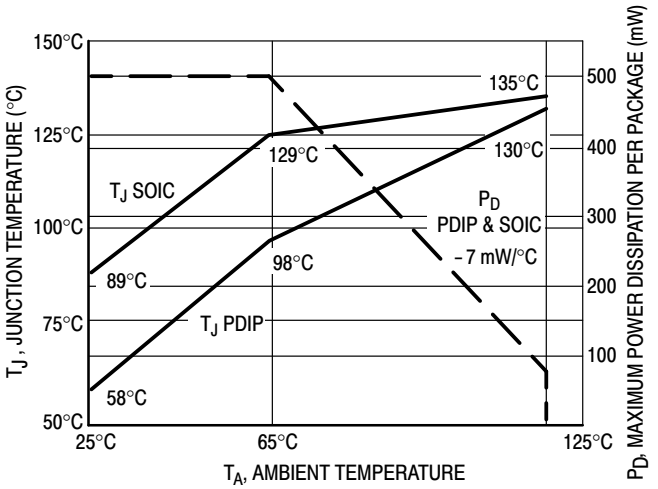


Figure 71. Junction Temperature for Typical CMOS Logic Device

This graph illustrates junction temperature for the worst case CMOS Logic device (MC14007UB) — smallest die area operating at maximum power dissipation limit in still air. The solid line indicates the junction temperature, T_J, in a Dual−In−Line (PDIP) package and in a Small Outline IC (SOIC) package versus ambient temperature, T_A. The dotted line indicates maximum allowable power dissipation derated over the ambient temperature range, 25°C to 125°C.

This graph illustrates junction temperature for a CMOS Logic device (MC14053B) — average die area operating at maximum power dissipation limit in still air. The solid line indicates the junction temperature, T_J, in a Dual−In−Line (PDIP) package and in a Small Outline IC (SOIC) package versus ambient temperature, T_A. The dotted line indicates maximum allowable power dissipation derated over the ambient temperature range, 25°C to 125°C.

STATISTICAL PROCESS CONTROL

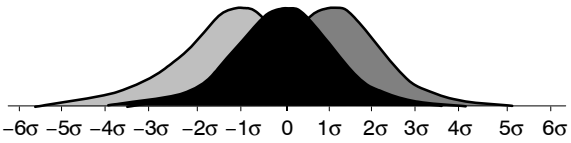
ON Semiconductor is continually pursuing new ways to improve product quality. Initial design improvement is one method that can be used to produce a superior product. Equally important to outgoing product quality is the ability to produce product that consistently conforms to specification. Process variability is the basic enemy of semiconductor manufacturing since it leads to product variability. Used in all phases of ON Semiconductor's product manufacturing, STATISTICAL PROCESS CONTROL (SPC) replaces variability with predictability. The traditional philosophy in the semiconductor industry has been adherence to the data sheet specification. Using SPC methods ensures that the product will meet specific process requirements throughout the manufacturing cycle. The emphasis is on defect prevention, not detection. Predictability through SPC methods requires the manufacturing culture to focus on constant and permanent improvements. Usually, these improvements cannot be bought with state−of−the−art equipment or automated factories. With quality in design, process, and material selection, coupled with manufacturing predictability, ON Semiconductor can produce world class products.

The immediate effect of SPC manufacturing is predictability through process controls. Product centered and distributed well within the product specification benefits ON Semiconductor with fewer rejects, improved yields, and lower cost. The direct benefit to ON Semiconductor's customers includes better incoming quality levels, less inspection time, and ship−to−stock capability. Circuit performance is often dependent on the cumulative effect of component variability. Tightly controlled component distributions give the customer greater circuit predictability. Many customers are also converting to just−in−time (JIT) delivery programs. These programs require improvements in cycle time and yield predictability achievable only through SPC techniques. The benefit derived from SPC helps the manufacturer meet the customer's expectations of higher quality and lower cost product.

Ultimately, ON Semiconductor will have Six Sigma capability on all products. This means parametric distributions will be centered within the specification limits, with a product distribution of plus or minus Six Sigma about mean. Six Sigma capability, shown graphically in Figure 72, details the benefit in terms of yield and outgoing quality levels. This compares a centered distribution versus a 1.5 sigma worst case distribution shift.

New product development at ON Semiconductor requires more robust design features that make them less sensitive to minor variations in processing. These features make the implementation of SPC much easier.

A complete commitment to SPC is present throughout ON Semiconductor. All managers, engineers, production operators, supervisors, and maintenance personnel have received multiple training courses on SPC techniques. Manufacturing has identified 22 wafer processing and 8 assembly steps considered critical to the processing of semiconductor products. Processes controlled by SPC methods that have shown significant improvement are in the diffusion, photolithography, and metallization areas.



Standard Deviations From Mean

Distribution Centered	Distribution Shifted ± 1.5
At ± 3σ 2700 ppm defective 99.73% yield	66810 ppm defective 93.32% yield
At ± 4σ 63 ppm defective 99.9937% yield	6210 ppm defective 99.379% yield
At ± 5σ 0.57 ppm defective 99.999943% yield	233 ppm defective 99.9767% yield
At ± 6σ 0.002 ppm defective 99.9999998% yield	3.4 ppm defective 99.99966% yield

Figure 72. AOQL and Yield from a Normal Distribution of Product With 6σ Capability

To better understand SPC principles, brief explanations have been provided. These cover process capability, implementation, and use.

PROCESS CAPABILITY

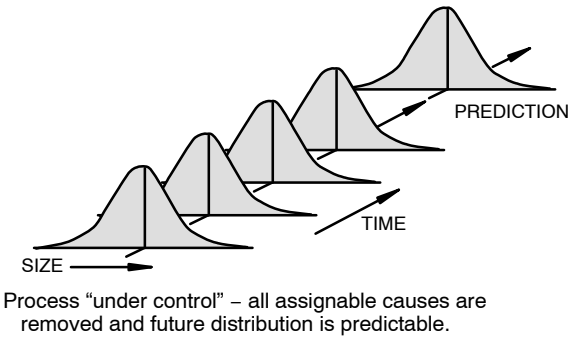
One goal of SPC is to ensure a process is **CAPABLE**. Process capability is the measurement of a process to produce products consistently to specification requirements. The purpose of a process capability study is to separate the inherent **RANDOM VARIABILITY** from **ASSIGNABLE CAUSES**. Once completed, steps are taken to identify and eliminate the most significant assignable causes. Random variability is generally present in the system and does not fluctuate. Sometimes, the random variability is due to basic limitations associated with the machinery, materials, personnel skills, or manufacturing methods. Assignable cause inconsistencies relate to time variations in yield, performance, or reliability.

Traditionally, assignable causes appear to be random due to the lack of close examination or analysis. Figure 73 shows the impact on predictability that assignable cause can have. Figure 74 shows the difference between process control and process capability.

A process capability study involves taking periodic samples from the process under controlled conditions. The performance characteristics of these samples are charted against time. In time, assignable causes can be identified and engineered out. Careful documentation of the process is the key to accurate diagnosis and successful removal of the

assignable causes. Sometimes, the assignable causes will remain unclear, requiring prolonged experimentation.

Elements which measure process variation control and capability are Cp and Cpk, respectively. Cp is the specification width divided by the process width or Cp = (specification width) / 6σ. Cpk is the absolute value of the closest specification value to the mean, minus the mean, divided by half the process width or Cpk = | closest specification − $\overline{X}$/3σ.



Process “under control” − all assignable causes are removed and future distribution is predictable.

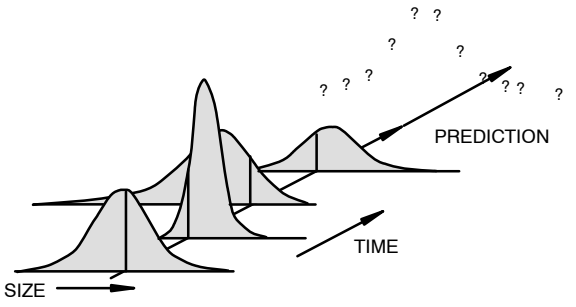
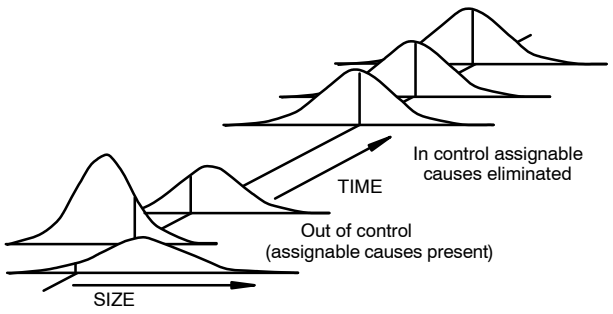


Figure 73. Impact of Assignable Causes on Process Predictable



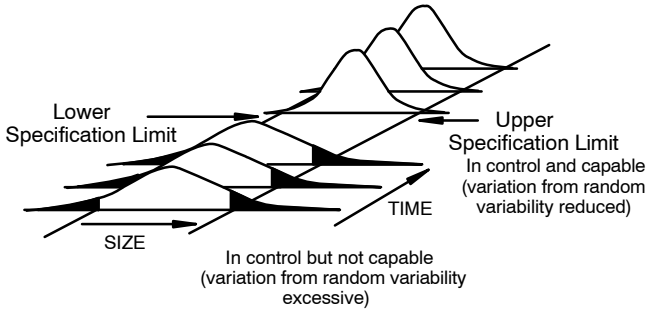


Figure 74. Difference Between Process Control and Process Capability

At ON Semiconductor, for critical parameters, the process capability is acceptable with a Cpk = 1.50 with continual improvement our goal. The desired process capability is a Cpk = 2 and the ideal is a Cpk = 5. Cpk, by definition, shows where the current production process fits with relationship to the specification limits. Off center distributions or excessive process variability will result in less than optimum conditions.

SPC IMPLEMENTATION AND USE

CPSTG uses many parameters that show conformance to specification. Some parameters are sensitive to process variations while others remain constant for a given product line. Often, specific parameters are influenced when changes to other parameters occur. It is both impractical and unnecessary to monitor all parameters using SPC methods. Only critical parameters that are sensitive to process variability are chosen for SPC monitoring. The process steps affecting these critical parameters must be identified as well. It is equally important to find a measurement in these process steps that correlates with product performance. This measurement is called a critical process parameter.

Once the critical process parameters are selected, a sample plan must be determined. The samples used for measurement are organized into **RATIONAL SUBGROUPS** of approximately two to five pieces. The subgroup size should be such that variation among the samples within the subgroup remain small. All samples must come from the same source e.g., the same mold press operator, etc. Subgroup data should be collected at appropriate time intervals to detect variations in the process. As the process begins to show improved stability, the interval may be increased. The data collected must be carefully documented and maintained for later correlation. Examples of common documentation entries are operator, machine, time, settings, product type, etc.

Once the plan is established, data collection may begin. The data collected with generate $\overline{X}$ and R values that are plotted with respect to time. $\overline{X}$ refers to the mean of the values within a given subgroup, while R is the range or greatest value minus least value. When approximately 20 or more $\overline{X}$ and R values have been generated, the average of these values is computed as follows:

$$X = (\overline{X} + \overline{X}2 + \overline{X}3 + \ldots)/K$$
$$\overline{R} = (R1 + R2 + R2 + \ldots)/K$$

where K = the number of subgroups measured.

The values of X and $\overline{R}$ are used to create the process control chart. Control charts are the primary SPC tool used to signal a problem. Shown in Figure 75, process control charts show $\overline{X}$ and R values with respect to time and concerning reference to upper and lower control limit values. Control limits are computed as follows:

R upper control limit = $UCL_R = D4\ \overline{R}$
R lower control limit = $LCL_R = D3\ \overline{R}$
$\overline{X}$ upper control limit = $UCL_{\overline{X}} = X + A2\ \overline{R}$
$\overline{X}$ lower control limit = $LCL_{\overline{X}} = X - A2\ \overline{R}$

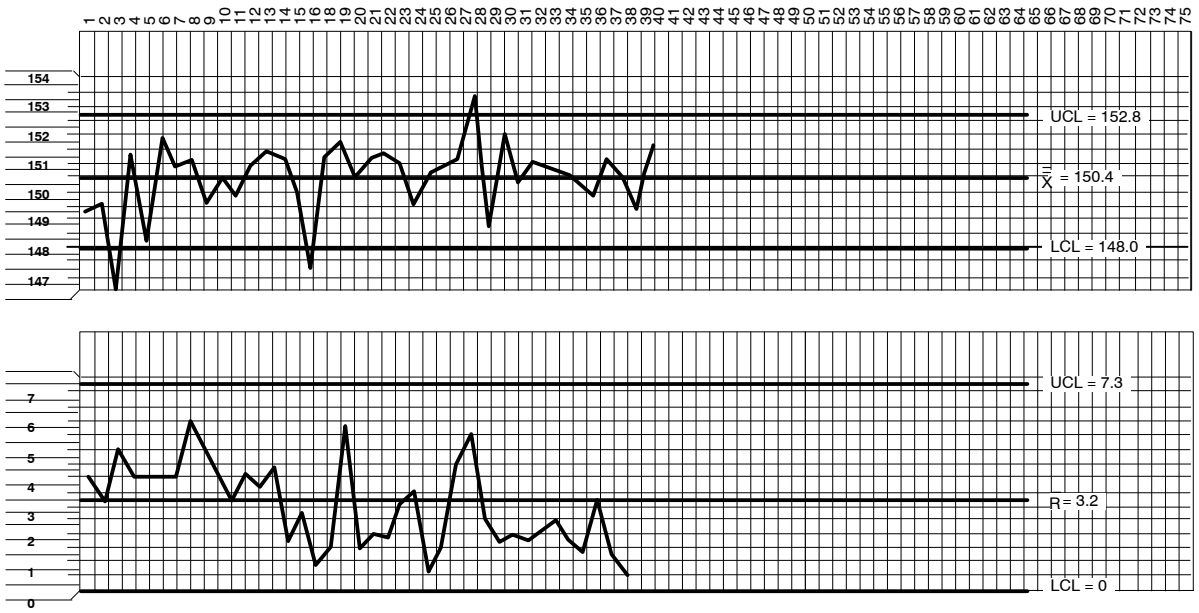


Figure 75. Example of Process Control Chart Showing Oven Temperature Data

Where D4, D3, and A2 are constants varying by sample size, with values for sample sizes from 2 to 10 shown in the following partial table:

n	2	3	4	5	6	7	8	9	10
D_4	3.27	2.57	2.28	2.11	2.00	1.92	1.86	1.82	1.78
D_3	*	*	*	*	*	0.8	0.14	0.18	0.22
A_2	1.88	1.02	0.73	0.58	0.48	0.42	0.37	0.34	0.31

*For sample sizes below 7, the LCL_R would technically be a negative number; in those cases there is no lower control limit; this means that for a subgroup size 6, six “identical” measurements would not be unreasonable.

Control charts are used to monitor the variability of critical process parameters. The R chart shows basic problems with piece to piece variability related to the process. The X chart can often identify changes in people, machines, methods, etc. The source of the variability can be difficult to find and may require experimental design techniques to identify assignable causes.

Some general rules have been established to help determine when a process is **OUT–OF–CONTROL**. Figure 76 shows a control chart subdivided into zones A, B, and C corresponding to 3 sigma, 2 sigma, and 1 sigma limits respectively. In Figures 77 through 80 four of the tests that can be used to identify excessive variability and the presence of assignable causes are shown. As familiarity with a given process increases, more subtle tests may be employed successfully.

Once the variability is identified, the cause of the variability must be determined. Normally, only a few factors have a significant impact on the total variability of the process. The importance of correctly identifying these factors is stressed in the following example. Suppose a process variability depends on the variance of five factors A, B, C, D, and E. Each has a variance of 5, 3, 2, 1, and 0.4, respectively.
Since:

$$\sigma\ tot = \sqrt{\sigma A^2 + \sigma B^2 + \sigma C^2 + \sigma D^2 + \sigma E^2}$$

$$\sigma\ tot = \sqrt{5^2 + 3^2 + 2^2 + 1^2 + (0.4)^2} = 6.3$$

If only D is identified and eliminated, then:

$$\sigma\ tot = \sqrt{5^2 + 3^2 + 2^2 + (0.4)^2} = 6.2$$

This results in less than 2% total variability improvement. If B, C, and D were eliminated, then:

$$\sigma\ tot = \sqrt{5^2 + (0.4)^2} = 5.02$$

This gives a considerably better improvement of 23%. If only A is identified and reduced from 5 to 2, then:

$$\sigma\ tot = \sqrt{2^2 + 3^2 + 2^2 + 1^2 + (0.4)^2} = 4.3$$

Identifying and improving the variability from 5 to 2 yields a total variability improvement of nearly 40%.

Most techniques may be employed to identify the primary assignable cause(s). Out–of–control conditions may be correlated to documented process changes. The product may be analyzed in detail using best versus worst part comparisons or Product Analysis Lab equipment. Multi–variance analysis can be used to determine the family of variation (positional, critical, or temporal). Lastly, experiments may be run to test theoretical or factorial analysis. Whatever method is used, assignable causes must be identified and eliminated in the most expeditious manner possible.

After assignable causes have been eliminated, new control limits are calculated to provide a more challenging variability criteria for the process. As yields and variability improve, it may become more difficult to detect improvements because they become much smaller. When all assignable causes have been eliminated and the points remain within control limits for 25 groups, the process is said to in a state of control.

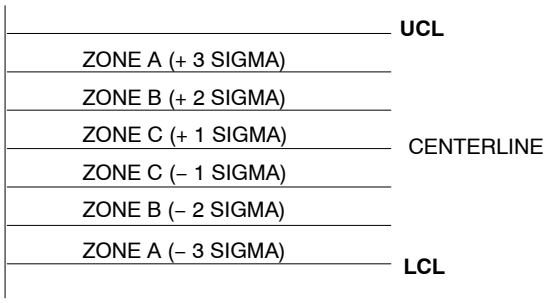


Figure 76. Control Chart Zones

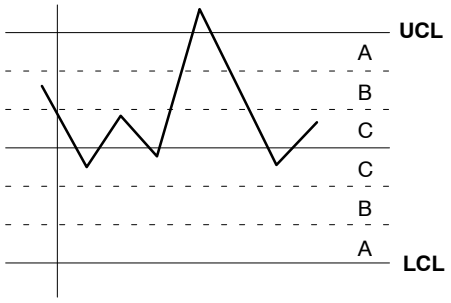


Figure 77. One Point Outside Control Limit Indicating Excessive Variability

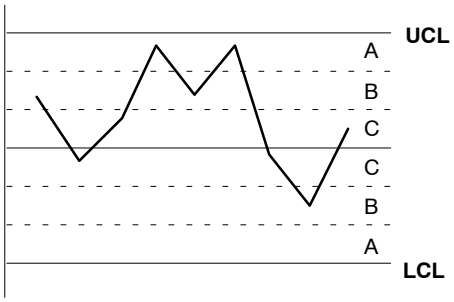


Figure 78. Two Out of Three Points in Zone A or Beyond Indicating Excessive Variability

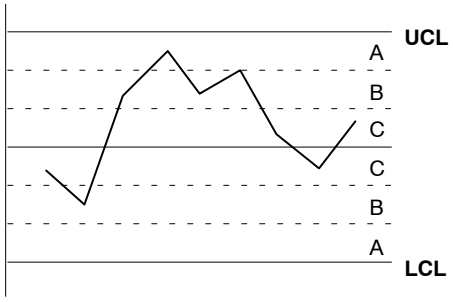


Figure 79. Four Out of Five Points in Zone B or Beyond Indicating Excessive Variability

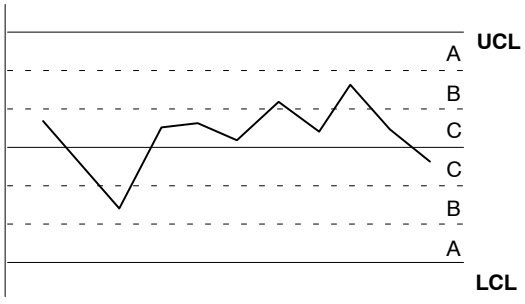


Figure 80. Seven Out of Eight Points in Zone C or Beyond Indicating Excessive Variability

SUMMARY

ON Semiconductor is committed to the use of STATISTICAL PROCESS CONTROLS. These principles, used throughout manufacturing have already resulted in many significant improvements to the processes. Continued dedication to the SPC culture will allow ON Semiconductor to reach the Six Sigma and zero defect capability goals. SPC will further enhance the commitment to **TOTAL CUSTOMER SATISFACTION**.

Section 5

Device Rework / Removal

Device Rework/Removal

Objective

The objective of this information brief is to provide the customer with a general understanding of the basic methods and risks associated with second level (board level) rework and device removal of surface mount components. This information brief outlines the basic requirements for assembly handling and preparation with particular attention paid to moisture-induced failure modes known as “popcorning”.

For detailed specifics on rework and removal processes and procedures refer to IPC-7711A/7721A, Rework of Electronic Assemblies, and Repair and Modification of Printed Boards and Electronic Assemblies[1].

Introduction

The soldering of surface mount ICs on application boards is a well-established process in the microelectronics industry. One well-known issue during surface mount re-flow is the potential for structural damage to the product during high temperature excursions due to residual moisture present in the package (popcorning). The phenomenon and risks associated with popcorning have been understood for decades and have been minimized by proper implementation of product moisture level classifications and appropriate product handling. These tests and definitions are defined by the internationally accepted industry standards IPC/JEDEC J-STD-020C, Moisture/ Re-flow Moisture Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices[2].

Background on Popcorn Failure Modes

The majority of electronic packaging today incorporates the use of polymer epoxies for various functions. Typical printed circuit boards (PCB) use a glass weave impregnated with an epoxy resin. Microelectronic packages use epoxy die attach material and a resin-based encapsulation material. It is known that nearly all polymers are transmissive to water in the vapor form. Generally polymer-based microelectronics devices will, when subjected to moisture, allow water vapors to penetrate and accumulate within the package. The moisture will reside within the bulk polymer and also at interfaces within the package (die to leadframe, leadframe to overmold, etc). Upon high temperature excursions, such as solder re-flow during board-level assembly, the moisture within these packages will rapidly expand and result in destructive forces within the package. These forces have the ability to cause catastrophic damage in the devices (see Figure 81). Possible failure modes that may occur due to excess moisture absorption and/or excess temperature:

At the IC level:

- Delamination / pop-corning
- Open contacts
- Damaged, broken or bended leads
- EOS damage
- Damaged or removed solder pads on BGAs

At the board level:

- Open contacts
- EOS damage
- Damaged or removed solder pads
- Damaged or destroyed surrounding parts
- Damaged or destroyed application board

This damage can be made evident by various methods such as:

- External visual inspection for cracks and/or bulges in the package.
- Acoustic scan for areas of interfacial delamination.
- Cross-section through delaminated areas.
- Electrical tests exhibiting open contacts.

[1] IPC-7711A/7721A, Rework of Electronic Assemblies, February 2002 and Repair and Modification of Printed Boards and Electronic Assemblies, April 2001.

2 IPC/JEDEC J-STD-020C, Moisture/Re-flow Moisture Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices, July 2004.

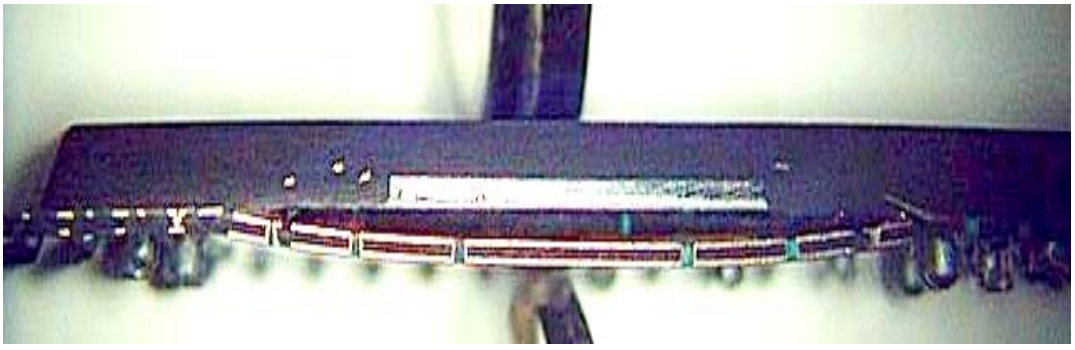


Figure 81. BGA Cross Section Exhibiting Moisture Damage (Popcorning)

Background on MSL Levels

Standard IPC/JEDEC J-STD-020C, Moisture/Re-flow Moisture Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices, was developed to address proper product handling to minimize the potential for moisture-induced failures during customer assembly. In support of these IPC/JEDEC standards, AMIS has performed extensive testing across package platforms. The testing included:

- Moisture absorption/ desorption characterization
- Moisture sensitivity level testing (MSL)

Moisture absorption/desorption testing is performed to understand the dynamic characteristics of the polymer when exposed to moisture and/or heat. Moisture desorption curves are particularly important as they provide measurement data to ensure products are fully desorbed prior to dry pack and shipment. Desorption provides the customer with product free of entrapped moisture. Figure 82 gives a typical desorption curve of QFP 28x28. Above the 0.05 percent level a package is considered to be vulnerable to popcorning.

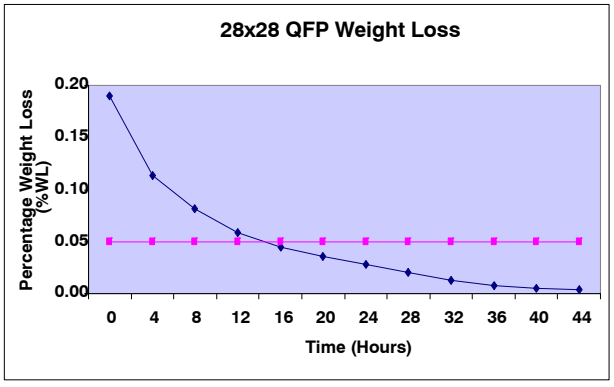


Figure 82. Weight Loss Profile Example

MSL levels are used to classify the sensitivity of a microelectronic package to moisture. Packages can be classified from level 1 (hermetic package) to level 6 (very sensitive). Note that Maximum Allowed Floor Life Before Soldering is the time from which the package has been exposed to ambient conditions. Knowledge of the appropriate MSL level of a package is crucial during second level solder re-flow, rework or part removal as the level dictates the duration that the package can be exposed to the atmosphere before being exposed to solder re-flow temperatures. Once this time limit expires, the package is at risk for catastrophic damage during any high temperature excursions. summarizes the different MSL levels as defined by JEDEC Standard J-STD-020C[ii].

Table 1: Moisture Sensitivity Levels by JEDEC

Level	Maximum Allowed Floor Life Before Soldering
1	Unlimited
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Time on label

Product Maximum Temperature Capabilities

Table 2 and Table 3 summarize peak temperature capabilities based upon the product dimensions and whether the application will use lead-based or lead-free solder materials[ii]. For more details, reference IPC/JEDEC J-STD-020C, Moisture/Reflow Moisture Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices, July 2004.

Table 2: Peak Temperature Capabilities, SnPb Eutectic

Package Thickness (mm)	Volume (mm^3) >350	Volume (mm^3) ≥350
<2.5	240 + 0/-5C	225 + 0/-5C
≥2.5	225 + 0/-5C	225 + 0/-5C

Table 3: Peak Temperature Capabilities, Pb-Free

Package Thickness (mm)	Volume (mm^3) >350	Volume (mm^3) 350 - 2000	Volume (mm^3) ≥2000
<1.6	260 + 0C	260 + 0C	260 + 0C
1.6 – 2.5	260 + 0C	250 + 0C	245 + 0C
≥2.5	250 + 0C	245 + 0C	245 + 0C

Product Rework/Removal Goals[i]

The product removal/rework process should be defined so as to minimize damage to the removed device, the replacement device and the surrounding components and board. Generally, the following guidelines are critical to successful rework/removal.

- Pre-auxiliary heat assembly and/or component if required.
- Evenly apply heat in a rapid, controllable fashion to achieve complete, simultaneous reflow of all solder joints.
- Avoid thermal and/or mechanical damage to component, board, adjacent components and their joints.

- Immediately remove component from board before any solder joint re-solidifies.
- Properly desorbing the components and assembly is critical to reduce the risk of moisture-induced failures.

Cleaning[ii]

Surface contaminants can significantly affect soldering, bonding, coating, and the electrical characteristics of the assembly. All foreign materials like stickers or conformal coatings should be removed from the device prior to exposure to temperature. Any use of mechanical force should be avoided. The board manufacturer should be contacted for the optimum process to remove the conformal coating when applied and other foreign materials. Reference IPC771A/7721A, number 2.2 for details.

Coating Removal[ii]

IPC771A/7721A, number 2.3 covers techniques for identifying various coatings so the appropriate removal technique can be selected. There are three removal methods outlined.

- Paragraph 2.3.2 is a procedure for coating removal using solvents
- Paragraph 2.3.3 outlines coating removal using a peel method typically used to remove silicone or rubbery coatings
- Paragraph 2.3.4 outlines a thermal removal
- Paragraph 2.3.5 outlines a grinding/scraping method
- Paragraph 2.3.6 outlines a microblasting method

Moisture Desorption

This is a very important step to ensure the board, surrounding components and the targeted components are not damaged in the rework/replacement process. Before the rework or removal can take place all residual moisture inherent in the assembly should be eliminated using a dry bake process. Although IPC771A/7721A provides little information on this process, minimal time temperature exposure can be empirically determined using weight-gain measurements. If this information is not available, a general rule of thumb is to perform a 24-hour bake at 125°C. Be aware that some parts on the application board may not be able to withstand the peak temperature of 125°C. These are parts like connectors, some capacitor types, coils, etc. Suppliers should be contacted to identify the maximum allowed temperatures for these components. In the event of potential damage at 125°C, an alternate lower temperature process is 96 hours at 50°C/10%RH.

Preheat/Auxiliary Heat[ii]

Preheat is used when:

- There is a risk of thermal shock to the substrate, components or both
- The primary heating method cannot bring all of the solder joints completely up to the proper re-flow temperature at all, or in an acceptable time

Preheating is typically performed from the bottom side of the assembly by use of a controlled conduction heat plate, a controlled convection heat device or a system utilizing both.

Product Rework/Removal

Because of the complexity involved in physically reworking electronic assemblies, refer to IPC-7711A/7721A, Rework of Electronic Assemblies, and Repair and Modification of Printed Boards and Electronic Assemblies for details in methods. It is highly recommended that personnel performing rework be trained in the appropriate skills and knowledge to meet this IPC specification.

The following recommendations are provided:

- The use of a soldering iron should be avoided, as it is very difficult to maintain temperatures across all leads simultaneously.
- Maximum allowed time at peak temperature should not be exceeded.
- Use of vacuum pinchet is advised.
- Excessive mechanical force should be avoided.
- All actions should be taken to avoid ESD/EOS damage of the parts during the handling and rework/removal operation.

Storage

Because the application board will immediately begin to absorb moisture upon exposure to ambient conditions, the time between removal from the dry oven and the de-soldering should be kept as short as possible. If this exposure time cannot be limited to a few hours, it is advised that the board be stored in a dry nitrogen environment to prevent further absorption.

Lead-free Solders[ii]

Although similar to rework of lead-based solders, there are some significant differences when using lead-free solders that need to be noted:

- The new alloys will require more time and higher temperatures to re-flow adequately. This may increase oxidation.
- Because the melting points are higher, there may be the need for modified flux chemistry.
- Wetting times are longer.
- Standard solderability visual indicators will be different (wetting angles, joint appearance).

Shipping and Transport

Shipping and transport of parts within or outside the company is important. ESD/EOS precautions should be taken. It is advised to move the parts in boxes with anti-static foam to avoid ESD/EOS events and to avoid mechanical damage. Parts should not be allowed to come into contact with each other to avoid mechanical damage during transport.

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